CAD-ORIENTED ANALYTIC FORMULAS FOR CAPACITANCE MATRIX OF INTERCONNECTS ON LOSSY SILICON SUBSTRATE

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SUMMARY

A set of closed-form expressions is derived for the capacitance per unit length of the most common two-dimensional VLSI interconnect structures. The results have been obtained by using an approximate electromagnetic analysis of two coupled interconnect conductors over a ground plane (silicon substrate). We assume that the electric field meets the boundary conditions of a single isolated infinite line; therefore the boundary conditions for the conductors in the structure are approximately satisfied. It is shown by the numerical results that the derived formulas in this paper can provide an easy-to-use and fast-to-compute solver that results in accurate and reliable capacitance per unit length values.

1. INTRODUCTION

In modern analogue and digital IC's, interconnections are the main source of the overall delay. Moreover, the proximity of the interconnects can induce serious crosstalk issues. In advanced IC technologies, where the interconnection pitch is less than 2 μm (i.e., the spacing is close to or less than 1 μm), the line-to-line capacitance per unit length is comparable to or larger than the line-to-ground capacitance per unit length. Nowdays many efforts are being devoted to develop numerical, approximate analytical or in some simple topologies exact solutions to deal with the analysis of the three-dimensional interconnect configurations. There are a couple of procedures which can solve this problem numerically, for instance, finite difference or finite element approaches [1]. To this purpose, techniques based on the use of Green's functions were proposed in [2-5]. On the other hand, all numerical or seminumerical techniques are computationally expensive, so that run times risk to become prohibitive for VLSI layouts, even in the two-dimensional case. The same is true for the exact analytical solution, which is very difficult to derive and results in an extremely complicated modelling of even simple interconnect configurations.

The high accuracy expressions for capacitance of simple topologies, such as the single or double metal interconnects above a ground plane has been published by Chang [6], who used the conformal transformation method. If $w \geq h$ (w is conductor width and h is the line to ground plane distance) holds, their accuracy is within 1 % of the exact value. In [7], greatly simplified analytical expressions were proposed, where the 2-D structure was divided in elementary components like bottom, top and side wall contributions. In [8], Yuan and Trick derived some simple analytical expressions where the rectangular cross-section of the line was replaced by the oval one [9, 10].

In this work, a new approximate analytical formula for capacitance per unit length for VLSI interconnects is presented and verified. To calculate the capacitance of an interconnect it is assumed that the electric field is transverse to the axis of propagation. When we assume quasi-TEM mode of propagation an electrostatic analysis can be used to determine the potential distribution in the structure. The Green's function of the electric type is derived using the method of images. The self and mutual capacitance per unit length formulas proposed in this paper are calculated from the quasi-static charge matrix equation; these CAD-oriented closed-form expressions are suitable for a large range of line aspect ratios.

2. MODELING APPROACH

In order to properly analyze a periodic array of interconnect lines which have distributional characteristics, the system can be viewed as a coupled parallel conductor lines over a single perfectly conducting ground plane. In its most elemental form this structure consists of only two adjacent interconnect lines, as shown in Fig. 1. It should be noted that the coupling between two adjacent lines with the nearest neighbours is greater than the equivalent coupling that would occur in a periodic array, since field sharing would be expanded to include the other conductors in the configuration. Thus, the analysis of only two-coupled interconnect conductor lines would yield a good background for VLSI interconnect design purposes.

2.1 Two-dimensional Green's function for homogeneous dielectric medium

We consider first the potential produced by a unit line charge located at the source point $\mathbf{r_s} = (x_s, y_s)$ in a homogeneous dielectric medium with permittivity

$\varepsilon = \varepsilon_0\varepsilon_r$. This potential has the nature of a two-dimensional Greens function $G(\mathbf{r}_s: \mathbf{r}_f)$. The corresponding electric field is purely radial and can be calculated by an application of Gauss's law. Thus,

$$\mathbf{E}(\mathbf{r}_f) = \frac{1}{2\pi\varepsilon}\frac{\mathbf{r}_f - \mathbf{r}_s}{\left|\mathbf{r}_f - \mathbf{r}_s\right|^2} \tag{1}$$

where $\mathbf{r}_f = (x_f, y_f)$ is the field point in the xy plane.

The scalar Green's function of the problem satisfy the Poisson equation

$$\nabla^2 G(\mathbf{r}_s;\mathbf{r}_f) = -\frac{1}{\varepsilon}\delta(\mathbf{r}_f - \mathbf{r}_s) \tag{2}$$

and is given as

$$G(\mathbf{r}_f;\mathbf{r}_s) = \frac{1}{2\pi\varepsilon}\log\frac{1}{\left|\mathbf{r}_f - \mathbf{r}_s\right|}. \tag{3}$$

The potential distribution produced by a line charge of density Q_l is

$$\varphi(\mathbf{r}_f) = Q_l G(\mathbf{r}_f;\mathbf{r}_s)$$

or

$$\varphi(\mathbf{r}_f) = \frac{Q_l}{2\pi\varepsilon}\log\frac{1}{\left|\mathbf{r}_f - \mathbf{r}_s\right|} + const. \tag{4}$$

The potential at any point r_f with respect to a reference point $\mathbf{r}_R = (x_R, y_R)$ can be given as

$$\varphi(\mathbf{r}_f) - \varphi(\mathbf{r}_R) = \frac{Q_l}{2\pi\varepsilon}\log\frac{\left|\mathbf{r}_R - \mathbf{r}_s\right|}{\left|\mathbf{r}_f - \mathbf{r}_s\right|}, \tag{5}$$

where $\varphi(\mathbf{r}_R)$ is the potential of the reference point in the structure.

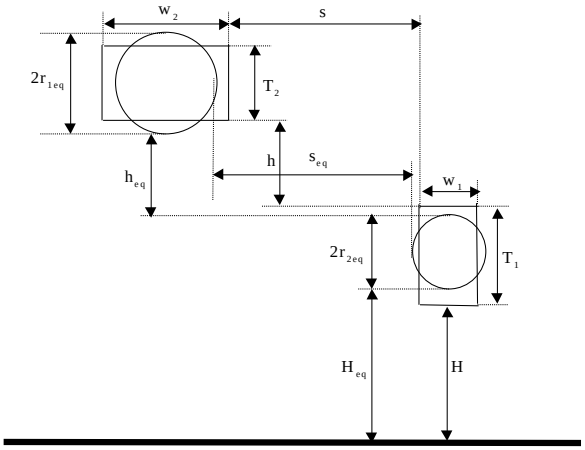

Fig. 1 Two rectangular conductors over a single ground plane and capacitance definitions (cross-section)

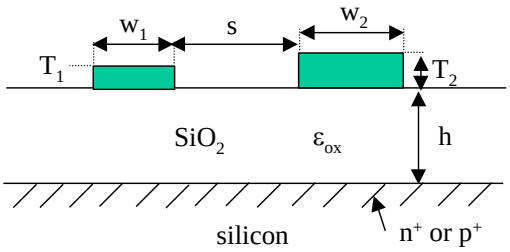

Fig. 2 The interconnect lines in a VLSI chip

2.2 Self and mutual capacitance formulas

The analysis of this representation of the coupled interconnect structure assumes only one mode of propagation (quasi-TEM). As a first step, round sectioned lines embedded in an electrically homogeneous medium are assumed, which is realistic for most microelectronic micrometre designs. This was found permissible (see numerical results) and simplifies the analysis considerably. The real and equivalent structure are shown in Fig.1, where the rectangular to circular conversion is used. To model actual rectangular conductors, we define an equaivalent diameter $2r_{ieq}$ (i = 1,2) as the mean of the diameters of the two circles inscribed in the conductors ($2r_{ieq} = (w_i + T_i)/2$)). The other geometrical dimensions h, H and s are consequently redefined as $H_{eq} = H + (T_2 - w_2)/4$, $h_{eq} = h + (T_1 - w_1)/4 + (T_2 - w_2)/4$, and $s_{eq} = s + (w_1 - T_1)/4 + (w_2 - T_2)/4$. The approach uses the fact that in a multiconductor system superposition may be used to determine the self and mutual capacitance per unit length from the electrostatic charge matrix equation. The charge-voltage relationships (capacitance matrix) can be expressed as follows:

$$\begin{bmatrix} Q_1 \\ Q_2 \end{bmatrix} = \begin{bmatrix} c_{11} & -c_{12} \\ -c_{21} & c_{22} \end{bmatrix}\begin{bmatrix} V_1 \\ V_2 \end{bmatrix}, \tag{6}$$

where Q_1 and Q_2 are the linear charge per unit length of each conductor, V_1 and V_2 are the potentials of each conductor, c_{11} and c_{22} are the self-capacitances per unit lenght of each conductor, and c_{12} and c_{21} are the mutual capacitance per unit length between conductors. For general configuration in Fig. 1, the self and mutual capacitances are

$$c_{11} = c_{g1} + c_m \tag{7a}$$

$$c_{22} = c_{g2} + c_m \tag{7b}$$

$$c_{12} = c_{21} = c_m. \tag{7c}$$

Using the equivalent structure shown in Fig. 1, where the rectangular to circular conversion can be applied, the coefficients c_{g1}, c_{g2}, c_m can be determined using quasi-static field analysis and method of images. The final closed-form expressions for the ground and mutual capacitances are given by

$$c_{g1} = \frac{2\pi\varepsilon \log\left[\dfrac{2h_2 - r_{2eq}}{r_{2eq}}\sqrt{\dfrac{d^2 + (h_2 - h_1 - r_{2eq})^2}{d^2 + (h_2 + h_1 - r_{2eq})^2}}\right]}{\log\left(\dfrac{2h_2 - r_{2eq}}{r_{2eq}}\right)\log\left[\dfrac{2h_1 - r_{1eq}}{r_{1eq}}\sqrt{\dfrac{d^2 + (h_1 - h_2 - r_{1eq})^2}{d^2 + (h_2 + h_1 - r_{1eq})^2}}\right] + \log\left(\sqrt{\dfrac{d^2 + (h_2 + h_1 - r_{1eq})^2}{d^2 + (h_1 - h_2 - r_{1eq})^2}}\right)A} \tag{8a}$$

$$c_{g2} = \frac{2\pi\varepsilon \log\left[\dfrac{2h_1 - r_{1eq}}{r_{1eq}}\sqrt{\dfrac{d^2 + (h_1 - h_2 - r_{1eq})^2}{d^2 + (h_2 + h_1 - r_{1eq})^2}}\right]}{\log\left(\dfrac{2h_2 - r_{2eq}}{r_{2eq}}\right)\log\left[\dfrac{2h_1 - r_{1eq}}{r_{1eq}}\sqrt{\dfrac{d^2 + (h_1 - h_2 - r_{1eq})^2}{d^2 + (h_2 + h_1 - r_{1eq})^2}}\right] + \log\left(\sqrt{\dfrac{d^2 + (h_2 + h_1 - r_{1eq})^2}{d^2 + (h_1 - h_2 - r_{1eq})^2}}\right)A} \tag{8b}$$

$$c_m = c_{g1}\frac{\log\sqrt{\dfrac{d^2 + (h_1 + h_2 - r_{1eq})^2}{d^2 + (h_1 - h_2 - r_{1eq})^2}}}{\log\left[\dfrac{2h_2 - r_{2eq}}{r_{2eq}}\sqrt{\dfrac{d^2 + (h_1 - h_2 - r_{1eq})^2}{d^2 + (h_2 + h_1 - r_{1eq})^2}}\right]} \tag{8c}$$

where $A = \log(((2h_2 - r_{2eq})/r_{2eq})\sqrt{(d^2 + (h_2 - h_1 - r_{2eq})^2)/(d^2 + (h_1 + h_2 - r_{2eq})^2)}$,

$h_2 = H_{eq} + r_{2eq}$ $h_1 = H_{eq} + h_{eq} + 2r_{2eq} + r_{1eq}$ and $d = s_{eq} + r_{1eq} + r_{2eq}$.

For the case of VLSI interconnects on an Si-SiO_2 substrate (Fig. 2) with a dielectric overlay (free space), it is convenient to assume that no dielectric interface exists and the total propagation medium is the homogeneous dielectric with relative effective permittivity

$$\varepsilon = \varepsilon_{eff}(\varepsilon_{ox}, h) = (\varepsilon_{ox} + 1)/2 + \left[(\varepsilon_{ox} - 1)(1 + 12h/w)^{-1/2}\right]/2 .$$

3. RESULTS

Let us consider a pair of coupled parallel interconnection lines embedded in a homogeneous medium over a ground plane as shown in Fig. 2.

The permittivity of the medium (silicon oxide) is $\varepsilon_{ox} = 3.9\varepsilon_0$. Table I provides a comparison of the line capacitances between data obtained by our analytical formulas and the data obtained by multilayer Green's function method [4] and electromagnetic solver (total charge boundary element method)[11], respectively. Good agreement between our results and the published data can be seen from Table 1. From the table we observe that there is a good agreement (difference less than 10 %) between our results and those obtained by quasi-analytical approach [4] or numerical oriented code [11].

	This paper		Green's function [4]		Quasi-static [11]	
w/H	C_{11}	C_{12}	C_{11}	C_{12}	C_{11}	C_{12}
0.5	7.580	-2.410	7.270	-2.370	7.270	-2.368
1.0	9.542	-1.839	9.219	-1.765	9.219	-1.766
1.25	10.592	-1.621	10.202	-1.584	10.200	-1.584
1.5	11.638	-1.312	11.149	-1.455	11.150	-1.454
2.0	13.971	-1.169	13.119	-1.278	13.120	-1.277
2.5	15.878	-1.214	15.044	-1.177	15.040	-1.176

Tab. 1 Self and mutual capacitance of a pair of coupled parallel interconnect lines with different geometries (10pF/m) with: $w_1 = w_2 = w$, $h = H_1 = H_2 = H$, $T_1 = T_2 = T$, w/s = 1, w/T = 1 and $\varepsilon_{ox} = 3.9\varepsilon_0$.

4. CONCLUSION

In this paper we have derived new expressions for the self and mutual capacitances of the most common 2-D VLSI interconnects. The capacitance elements have been obtained by the method of images in conjunction with the equivalent round cross-section of interconnect lines. The accuracy of the final results is validated with respect to the formulas and full-wave solvers already reported in literature.

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BIOGRAPHY

Hasan Ymeri was born in Druar near Mitrovicë, Kosovë on 24 October 1957. He received the Dipl. Ing. (M. Sc.) degree in electronic engineering from University of Prishtina, Prishtinë, Kosovë, in 1983, the Mag. Sci. degree in electrical engineering from the University of Ljubljana, Slovenia, in 1988, and the Dr. Sc. degree in electronic engineering from the Polytechnic University, Tirana, Albania, in 1996, respectively.
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