# ANALYSIS OF RECOVERY FROM COMMUTATION FAILURES IN AN HVDC INVERTER CONNECTED TO A WEAK RECEIVING AC SYSTEM

Mohamed KHATIR, Sid Ahmed ZIDI, Samir HADJERI, Mohammed Karim FELLAH
ICEPS Laboratory, Department of Electrical Engineering, Djillali Liabes University, PB 89 Sidi Bel Abbes 22000, Algeria, E-mails: med_khatir@yahoo.fr, sbzidi@yahoo.fr, shadjeri2@yahoo.fr, mkfellah@yahoo.fr

**ABSTRACT**

*The performance of an HVDC link is significantly impacted by the relative strength of the AC system to which it is connected. However, the interaction between AC and DC systems and the associated problems are very much dependent on the strength of the AC system relative to the capacity of the DC link. This paper explores the effect of the DC control on recovery from commutation failures in an HVDC inverter following AC system fault in line commutated thyristor inverter feeding a weak AC system. The AC system fault to which the study system is subjected is a single phase ground fault. MATLAB Simulink is used for the simulation studies.*

***Keywords:*** *HVDC transmission, commutation failures, recovery, VDCOL, short circuit ratio (SCR)*

## 1. INTRODUCTION

AC system faults in the electrical proximity of the inverter station causing inverter AC busbar voltage reductions in any or all phases may cause commutation failures in some or all of the connected valve groups. During the period of commutation failures, usually the fault duration, the associated valve groups cannot deliver any power into the AC network. The energy loss to the AC system during the fault is unavoidable [6, 9].

After fault clearing, the DC would normally be required to recover as quickly as possible to minimize the energy loss and prevent transient instability of the AC system. The importance of commutation failures during system faults, and therefore also the importance of commutation failure probability for remote faults in low and very low SCR systems, depends on the sensitivity of the receiving ac system to the energy deficit during the failure and the converter behaviour during the subsequent recovery period. If the recovery period is not smoothly controlled, the effects on the AC system can be aggravated.

The strength of the ac system is of course relative to the DC power or power rating of the connected DC converters. For a particular AC system, recovery from faults becomes more critical and difficult with increasing DC power injection. This is just another way of expressing that it is the SCR that is relevant. It is defined as [5, 7, 8]:

$$SCR = \frac{S}{P_{dc}} \tag{1}$$

$S$ is the short circuit capacity of the connected AC system in MVA, and $P_{dc}$ is the rating of the converter terminal in MW. The following SCR values can be used to classify an AC system [1]:

a) a strong AC system is categorized by an SCR ≥ 3.
b) a weak AC system is categorized by 2 ≤ SCR < 3.
c) a very weak AC system is categorized by an SCR < 2.

The most common failure type in an AC transmission network is a single-phase short circuit to earth, and we have therefore investigated only this type of fault.

## 2. DESCRIPTION OF THE EVENT

The basic module of an HVDC converter is the three-phase, full-wave bridge circuit shown in Fig. 1, where Va, Vb and Vc represent the AC side phase-voltage. $X_C$ is the commutating reactance of the external circuit. $I_d$ represents the DC side current. The circuit is known as Graetz Bridge.

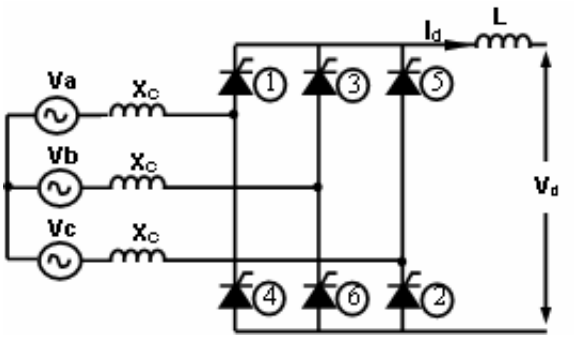


**Fig. 1** Equivalent circuit for three-phase full-wave bridge converter

Fig.2 shows the basic equivalent circuit of a line commutated converter, for which the process of commutation between valve 1 and valve 3 is illustrated. Under normal circumstances, the voltage across the valve being turned off has to remain negative for a certain period after the extinction of its current (denoted by the extinction angle γ in Fig. 3) so that it becomes capable of blocking the forward voltage. Should the valve voltage become positive prematurely, the valve may turn on even without a firing pulse, resulting in the failure of the commutation process.

Fig. 3 illustrates the angle relationships and angle definition for an inverter. During the commutation, the

two valves involved in the commutation (valve 1 and valve 3), conduct simultaneously and the phase-voltages in phase a and phase b will be short circuited through the two commutation reactance, $X_C$. Eventually, the current will be transferred from valve 1 to valve 3 and the commutation will be finished. The time this takes is measured by the commutation interval angle, or overlap angle, that is denoted μ. The volt-time area A, which is shown in fig.3, is required for the commutation.

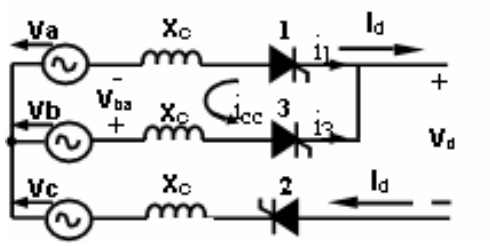


**Fig. 2** Basic equivalent circuit during the commutation

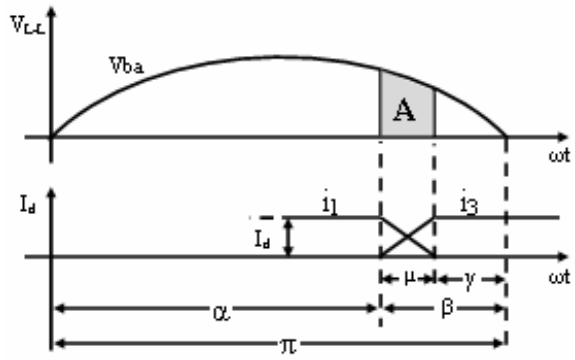


**Fig. 3** Commutation process between valve 1 and valve 3

During the commutation interval (μ), the total current $I_d$ is shifted from valve 1 to valve 3. At every instant:

$$I_d = i_1 + i_3 \tag{2}$$

and for $\alpha < \omega t < \alpha + \mu$ :

$$i_3 = \frac{I_d(\cos\alpha - \cos\omega t)}{\cos\alpha - \cos(\alpha + \mu)} \tag{3}$$

When a converter bridge is operating as an inverter, a valve will turn off when its forward current commutates to zero and the voltage across the valve remains negative. The period for which the valve stays negatively biased is the extinction angle γ, the duration beyond which the valve then becomes forward biased. Without a firing pulse, the valve will ideally stay non-conductive or blocked. The extinction angle γ depends on the angle of advance β and the angle of overlap μ and is determined by the relation:

$$\gamma = \beta - \mu \tag{4}$$

The angle of advance β is related in degrees to the angle of delay α by:

$$\beta = 180^o - \alpha \tag{5}$$

The delay angle α at the inverter may not be inherently known but once extinction angle γ and overlap angle μ have been determined, then:

$$\alpha = 180^o - (\gamma + \mu) \tag{6}$$

The μ commutation or overlap angle can be also calculated. Its theoretical value depends on α, the DC current Id and the commutation reactance $X_C$:

$$\mu = ar\cos\left[\cos(\alpha) - \frac{X_C I_d \sqrt{2}}{V_{LL}}\right] - \alpha \tag{7}$$

$V_{LL}$ is the line-to-line rms commutating voltage that is dependent on the AC system voltage and the transformer ratio.

The DC inverter therefore requires a minimum period of negative bias or minimum extinction angle γ for forward blocking to be successful. If forward blocking fails and conduction is initiated without a firing pulse, commutation failure occurs. This also results in an immediate failure to maintain current in the succeeding converter arm as the DC line current returns to the valve which was previously conducting and which has failed to sustain forward blocking.

Commutation failures at a converter bridge operating as an inverter are mainly caused by voltage dips due to AC system faults. Voltage dips may cause both voltage magnitude reduction and phase-angle shift. Voltage dips may affect the commutation in three ways [2, 3, 5]:

1- Increased DC current
2- Voltage magnitude reduction of the AC side
3- Phase angle shift

Fig. 4 [11] illustrates the dependence of the overlap angle μ compared to the delay angle α with the parameter ($I_d$ /$I_{ccM}$), where $I_{ccM}$ is the peak value of the current of short-circuit during the commutation interval (μ).

$$I_{ccM} = \frac{\sqrt{2}V_{LL}}{2X_C} \tag{8}$$

After some calculations, we have:

$$\cos(\alpha + \mu) = \cos\alpha - \frac{I_d}{I_{ccM}} \tag{9}$$

From the equation (9), we show that the overlap angle μ depends on the delay angle α and of the direct current $I_d$ to be commutated. The overlap angle μ increases with ($I_d$ /$I_{ccM}$), it becomes maximum for α = 0, this corresponds to operation of pure rectifier. If α increases, the overlap angle μ decreases, to reach a minimal value. For α > 90, μ

increases again, however a limit of operation exists by the fact that $\alpha + \mu < 180^o$.

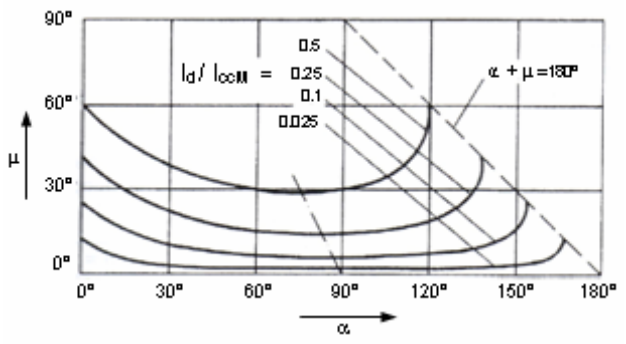


**Fig. 4** Variation of the overlap angle μ as a function of delay angle α

## 3. SYSTEM UNDER STUDY

A 1000 MW (500 kV, 2kA) DC interconnection is used to transmit power from a 500 kV, 5000 MVA, 60 Hz network (AC system 1, having a SCR of 5) to 345 kV, 2500 MVA, 50 Hz network (AC system 2, having a SCR of 2.5). The AC networks are represented by damped L-R equivalents with an angle of 80 degrees at fundamental frequency
(60 Hz or 50 Hz) and at the third harmonic. The rectifier and the inverter are 12-pulse converters using two universal bridge blocks connected in series. The converters are interconnected though a 300 km distributed parameter line and 0.5 H smoothing reactor. The converter transformer (Yg/Y/Δ) is modeled with three-phase transformer (three-Windings). The tap position is rather at a fixed position determined by a multiplication factor applied on the primary nominal voltage of the converter transformers (0.9 on rectifier side; 0.96 on inverter side).

The configuration of the system is given in fig. 5.

### 3.1. The AC systems

The AC networks, both at the rectifier and inverter end, are modeled as infinite sources separated from their respective commutating buses by system impedances. The impedances are represented as L-R/L networks having the same damping at the fundamental and the third harmonic frequencies. The impedance angles of the receiving end and the sending end systems are selected to be 80 degrees. This is likely to be more representative in the case of resonance at low frequencies [12].

### 3.2. DC system

The DC system is composed of smoothing reactors and a DC transmission line modeled with distributed parameter line with lumped losses [10]. This model is based on the Bergeron's traveling wave method used by the Electromagnetic Transient Program (EMTP).

### 3.3. The converter transformers

The 1200 MVA converter transformer is modeled with three-phase transformer (Three-Windings). The parameters adopted (based on AC rated conditions) are considered as typical for transformers found in HVDC installation such as leakage: $X_C = 0.24$ p.u

### 3.4. AC filters and capacitor banks

On AC side of 12-pulse HVDC converter, current harmonics of the order of 11, 13, 25 and higher are generated. Filters are installed in order to limit the amount of harmonics to the level required by the network. In the conversion process, the converter consumes reactive power, which is compensated in part by the filter banks and the rest by capacitor banks of 600 Mvar on each side.

### 3.5. Control systems

The rectifier and the inverter control both have a voltage and a current regulator operating in parallel calculating firing angle $\alpha_v$ and $\alpha_i$. Both regulators are of the proportional and integral type (PI).

In normal operation, the rectifier controls the current at the Id_ref reference value whereas the inverter controls the voltage at the Vd_ref reference value. The I_margin and Vd_margin parameters are respectively 0.1 p.u. and 0.05 p.u.

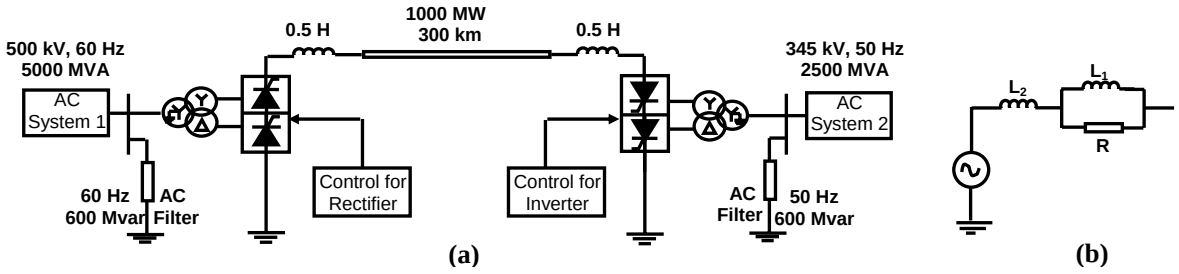


**Fig. 5** (a) HVDC System; (b) Details of AC system representation

*3.5.1. The VDCOL function*

Another important control function is implemented to change the reference current according to the value of the DC voltage. This control named Voltage Dependent Current Order Limits (VDCOL) automatically reduces the reference current (Id_ref) set point when VdL (Vd line) decreases (as for example, during a DC line fault or a severe AC fault). Reducing the Id reference currents also reduces the reactive power demand on AC network, helping to recover from fault [1,4]. The VDCOL parameters of the discrete 12-Pulse HVDC control are presented in figure 6.

The Id_ref value starts to decrease when the Vd line voltage falls bellow a threshold value VdThresh (0.6 p.u.). The actual reference current is named Id_ref-lim. IdMinAbs is the absolute minimum Id_ref set at 0.08 p.u. When the DC line voltage falls bellow the VdThresh value, the VDCOL reduces instantaneously Id_ref. However, when the DC voltage recovers, VDCOL limits the Id_ref rise time with a time constant defined by parameter (Tup).

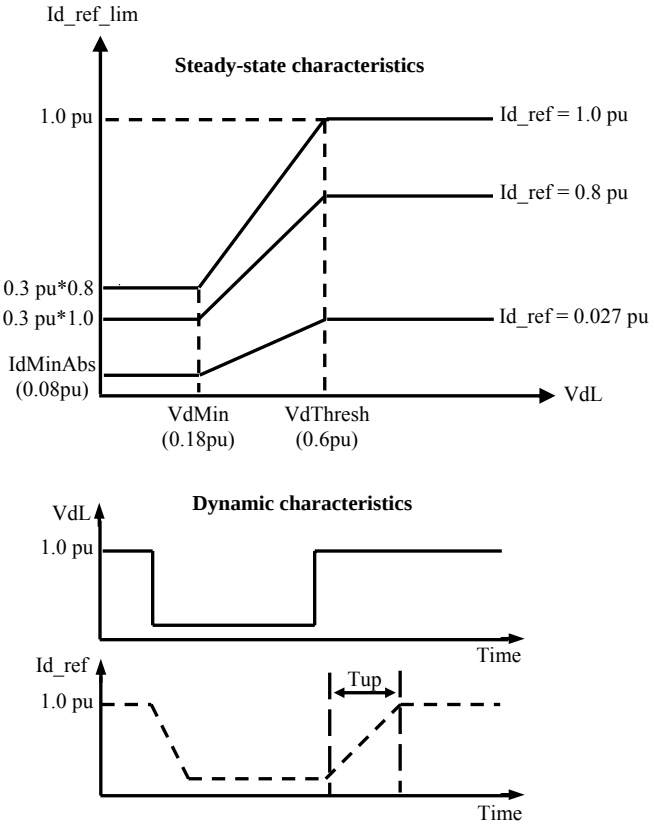


**Fig. 6** VDCOL Characteristics

## 4. SIMULATION RESULTS

For two different values of Tup (Id_ref rise time), a single phase-to-ground fault at inverter is examined in this article. For each of the transient case considered above, plots of rectifier and inverter DC current, DC voltage, and firing angle, are given. Also the inverter valves current of two Graetz bridges connected in series (The bridges are connected to the AC system by means of converter transformers, one of Y-Y winding structure and another Y-Δ winding structure, as shown in Fig.5).

### 4.1. Single phase-to-ground fault at inverter (Tup = 10 ms)

A single phase-to-ground fault was applied to the A-phase of the inverter bus, and the duration of the fault was 5 cycles, and the Id_ref rise time Tup = 10 ms. Results of this study are shown in fig.7 and fig.8.

When this fault is applied at t = 0.6 s, due to a reduction in AC voltage of the inverter bus, the inverter DC voltage decreases. The DC current therefore shoots up. The rectifier current controller attempts to reduce the current by increasing its firing angle and the rectifier therefore goes into the inverter region. The DC current decreases to a low average value as determined by VDCOL (0.3 pu).

From the fig.8, the inverter valves current plots indicate a number of commutation failures of the corresponding valve groups, which translates by an increase in the DC current because the valves 1 and 4 in the (YY) bridge are conducting current at the same time, and that the (YY) Graetz bridge is short-circuited on the DC side.

When the fault is cleared at t = 0.7 s, another commutation failure will accrue during the recovery in the second bridge (YΔ). Since the DC voltage is zero during a period following the commutation failure, no active power will be transmitted during this time. The system recovers in approximately 0.4 s after fault clearing.

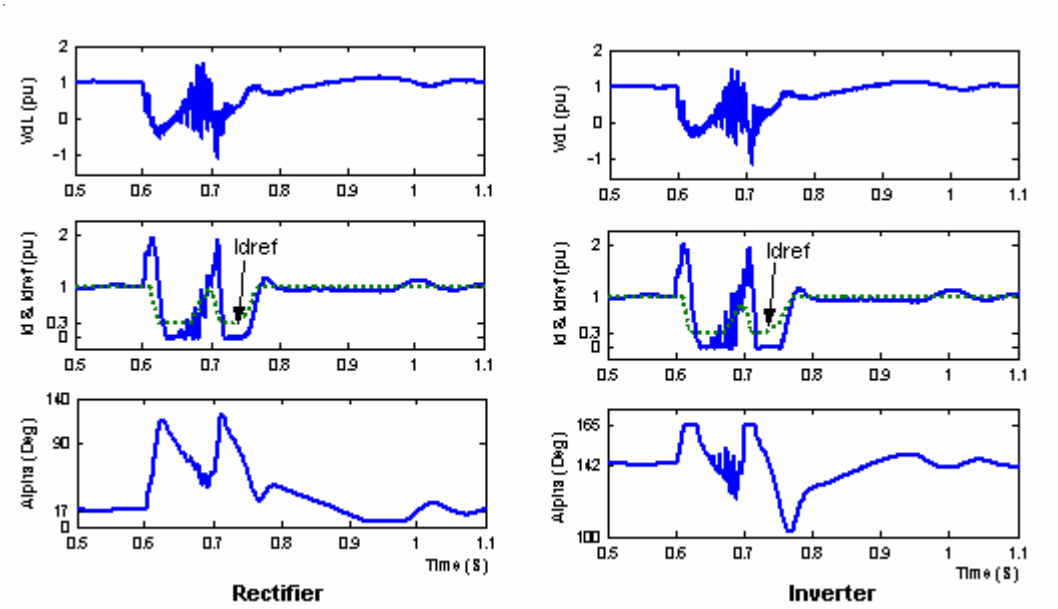


**Fig. 7** Single phase-to-ground fault at inverter (Tup = 10 ms)

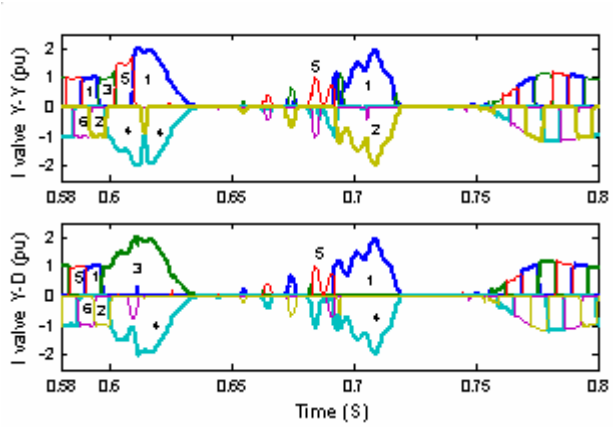


**Fig. 8** Inverter valves current during the fault (Tup = 10 ms)

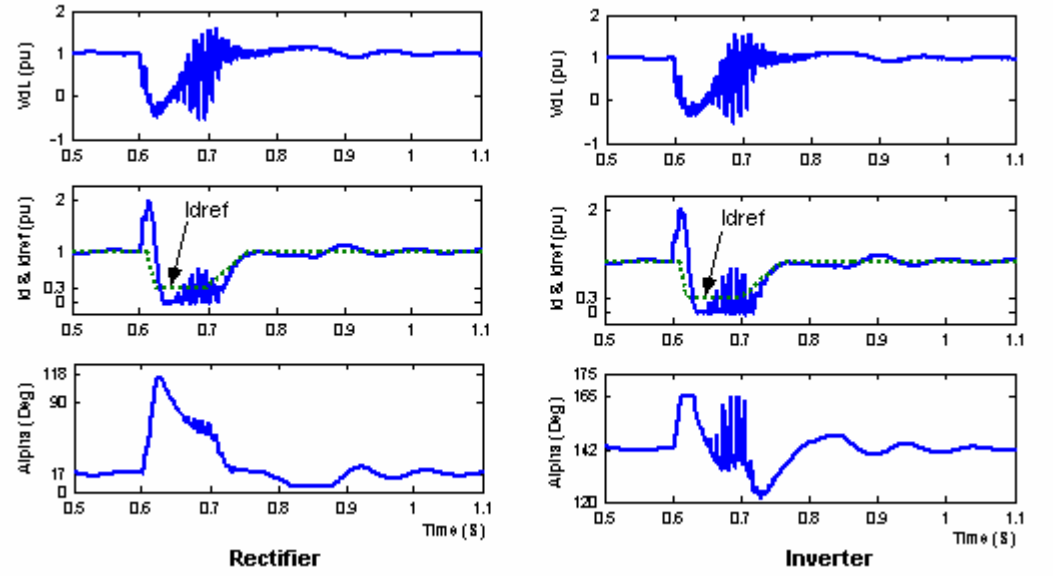


**Fig. 9** Single phase-to-ground fault at inverter (Tup = 80 ms)

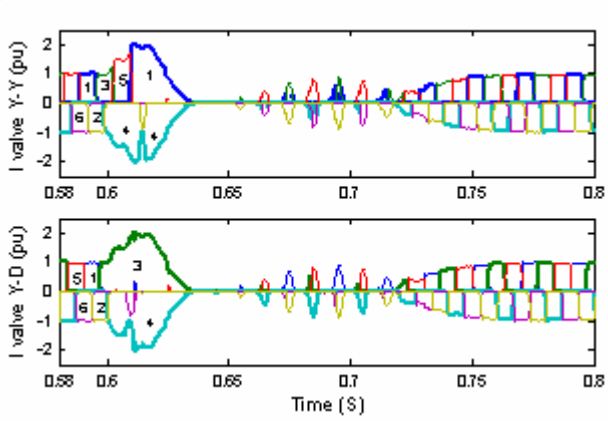


**Fig. 10** Inverter valves current during the fault (Tup = 80 ms)

### 4.2. Single phase-to-ground fault at inverter (Tup = 80 ms)

For the same fault, and a Tup = 80 ms, the waveforms resulting are displayed in Fig. 9 and 10. When this fault is applied at t = 0.6 s, commutation failure will accrue, and we can show that the valves 1 and 4 are conducting current at the same time, and that the (YY) Graetz bridge is short-circuited on the DC side. The DC current therefore shoots up; the VDCOL operates and reduces the reference current to 0.3 pu. When the fault is cleared at t = 0.7 s, the dc voltage starts to increase, following commutations take place in a normal way, and normal operation is resumed. The system recovers in approximately 0.3 s after fault clearing.

### 4.3. Discussion of the results

From the results given above results it is concluded that:

1. VDCOL function has an important role in determining the dc system recovery from commutation failure.
2. Following fault clearing, the VDCOL function current limit may be delayed and ramped so as to maximize the recovery rate while avoiding subsequent commutation failures.

## 5. CONCLUSION

To obtain good DC system recovery from commutation failure, control strategy alternatives can include delay or slow ramp recovery, reduced current level, and reduced power level at recovery (especially when the end system is disconnected due to some fault).

A voltage-dependent current order limit (VDCOL) function has an important role in determining the dc system recovery from faults, particularly from faults in a weak receiving-end ac system. The action of this function is to limit the current order as a function of the reduction in dc line voltage.

In the case of severe single line to ground faults, the VDCOL may also help to recover normal commutation and thus some power transfer can resume during the fault. Following fault clearing, the removal of the VDCOL function current limit may be delayed and ramped so as to maximize the recovery rate while avoiding subsequent commutation failures.

## REFERENCES

[1] Arrillaga, J : High Voltage Direct Current Transmission, ISBN 0-852969-41-4, The Institution of Electrical Engineers, 1998.

[2] Thio C.V, Davies J.B, Kent K.L: Commutation Failures in HVDC Systems, IEEE Trans. Power Delivery, vol. 11, no 2, Apr. 1996. pp. 946-957.

[3] Zou G, Jianchao Z, Xiangxum C: Study on Commutation Failure in an HVDC Inverter, IEEE Proce. POWERCON '98 on Volume 1, 18-21, Aug 1998. Page(s):503 – 506.

[4] Zidi S.A, Hadjeri S, Fellah M.K: Dynamic Performance of an HVDC Link, Journal of Electrical Systems, issue 1-3, 2005. pp 15-23.

[5] Thallam R S: Review of the Design and Performance Features of HVDC Systems Connected to Low Short Circuit Ratio AC Systems, IEEE Trans. Power Delivery, Vol. 7. No. 4.. October 1992. Page(s): 2065 – 2073

[6] Khatir M, Zidi S.A, Hadjeri S, Fellah M.K, Dahou O: The impact of AC system strength on commutation failures in an HVDC inverter, in proceeding of the 2nd International Conference on Electrical Systems, ICES'06, Oum El-Bouaghi, 8-10 may, 2006. Page (s): 369 - 374.

[7] Gavrilovic A, et al: Interaction between DC and AC Systems, Paper No. 200-20, CIGRE Symposium on AC/DC Transmission, Interactions and Comparisons, Boston (USA), September 1987.

[8] Gavrilovic A, et al: Some Aspects of AC/DC System Interaction, IEEE Montech '86, Conference on HVDC Transmission, Montreal, Canada

[9] Khatir M, Zidi S.A, Hadjeri S, Fellah M.K, Dahou O: Commutation failures in an HVDC inverter due to AC system faults, in proceedings of the International Conference on Electrical Engineering and its Applications, ICEEA'06, Sidi Bel-Abbès, 22-23 may, 2006.

[10] Zidi S.A : Contribution à l'étude des réseaux de transport d'énergie électrique CCHT en régime dynamique", doctorat thesis, Djillali Liabès university, Sidi Bel-Abbès, Alegria, 2005

[11] Seguier G : Les Convertisseurs de l'électronique de puissance, second édition, vol 1, Lavoisier-Tec & Doc, 1992

[12] Gole A. M: HVDC course notes, Manitoba HVDC Research Centre, Canada, 2000

Received August 21, 2006, accepted Jul 19, 2007

## BIOGRAPHIES

**Mohamed KHATIR** was born in Ain Temouchent, Algeria, in 1977. He received the Eng. degree in electro technical engineering, and the Master's degrees from the Djillali Liabes University of Sidi Bel Abbes (Algeria), in 2002 and 2006 respectively. He is now a PhD Candidate in the Electrical Engineering Department of Djillali Liabes University. His main field of interest includes HVDC and FACTS.

**Sid Ahmed ZIDI** was born in Sidi Bel Abbes, Algeria. He received the diploma of Electro technical Engineering degree from the university of Science and Technology of Oran, Algeria. The Master degree, from the university of Djillali Liabes of Sidi Bel-Abbes, Algeria in 1994. The PhD degrees from the university of Sidi Bel Abbes, Algeria, in 2005. He is currently interested by the HVDC link, FACTS and transient in power systems.

**Samir HADJERI** received the Master's degrees in Electrical Engineering from the university of Laval, Quebec, Canada, in 1990. The PhD degrees from the University of Sidi Bel-Abbes, Algeria, in 2003. Since 1991 he is a teaching member at the department of Electrical Engineering of Djillali Liabes University. His research there focused on HVDC, FACTS and power system analysis.

**Mohammed-Karim FELLAH** was born in Oran, Algeria, in 1963. He received the Eng. degree in Electrical Engineering from University of Sciences and Technology, Oran, Algeria, in 1986, and The Ph.D. degree from National Polytechnic Institute of Lorraine (Nancy, France) in 1991. Since 1992, he is Professor at the University of Sidi Bel Abbes (Algeria) and Director of the Intelligent Control and Electrical Power Systems Laboratory at this University. His current research interest includes power electronics, HVDC links, and drives.

## APPENDIX

Data for the system model:
Firing angle: $\alpha = 17^{\circ}$ (for the rectifier); $\alpha = 142^{\circ}$ (for the inverter).

***1- Rectifier end:*** The rectifier end AC system 1 representing a strong system (SCR = 5), consists of one source with an equivalent impedance of: $R = 26.07\ \Omega$, $L_1 = 48.86$ mH, $L_2 = 98.03$ mH.

***2- Inverter end:*** The inverter end AC system 2 representing a weak system SCR = 2.5, consists of one source with an equivalent impedance of: $R = 24.82\ \Omega$, $L_1 = 55.84$ mH, $L_2 = 112$ mH.

***3- DC line parameters:*** Rdc = 0.015 Ω/Km, L = 0.792 mH/km, C = 14.4 nF/km