ARCHITECTURE OF MULTI-CORE COMPUTER WITH DATA DRIVEN COMPUTATION MODEL

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ABSTRACT

Article describes tile computing paradigm and introduces representatives of tile computing computer architectures with control and data driven computation models and describes data flow computing paradigm. Article introduces architecture of computer with data driven computation model based on principles of tile computing which is the modern approach to multi-core design of microprocessors, with basic principle of cores layout in bi-directional mesh of cores with interconnecting communication network. Architecture is proposed on the Department of Computers and Informatics, Faculty of Electrical Engineering and Informatics, Technical University of Kosice. Hardware implementation of computers prototype with use of Xilinx Spartan 3 AN development board with Spartan 3 AN FPGA chip is also described.

Keywords: *tile computing, data flow computing, data driven architecture, data flow graph*

1. INTRODUCTION

Exponentially increasing amount of transistors integrated on the chip with increasing density of integration, in accordance to the Moore's law, provides opportunity to increase the performance of microprocessors.

Conventional superscalar architecture of microprocessor cannot be simply scaled up in line with this trend, and this situation results in challenging problem how to maintain continuity in proportion between quantity of integrated transistors and performance of the chip.

Disproportion between communication performance and computation performance intensifies with miniaturization of transistors, because of side effect of relative lengthening of inside chip wiring. Centralized control of microprocessor intensifies the problem. Memory model using cache memory causes extensive associative searches.

Increasing circuit complexity of superscalar microprocessors with longer design times, complex tests of designs and increasing amount of design bugs are also negative aspects of effort to increase the performance of superscalar microprocessors by integration of more transistors into single processor core.

Mainstream multi-core designs of superscalar processors are trying to address those challenges and commercially available microprocessors are integrating two or four cores into single chip.

2. TILE COMPUTING

Pushing trend in the architecture of multi-core microprocessors is integration of tens of cores in tiled configuration. Tile computing, introduced in [1], can be characterized by multiple use of processing elements, memory elements, input/output elements and various types of interconnecting networks. Proposed architectures are using control driven computation models also with VLIW and data driven computation models.

Representative of general purpose tile computing microprocessors is Tile64 designed by Tilera Corporation, described in [2]. Tile64 integrates 64 general purpose cores called tiles. Each core integrates L1 and L2 cache. Tiles are arranged in 8 × 8 bi-dimensional mesh using interconnecting network with 31Tbps data throughput. Chip utilizes 3-way VLIW pipeline for instruction level parallelism. Each tile is able to independently run operating system, or multiple tiles are able to run multiprocessing operating system. Performance of the chip at 700 MHz is 443.10^9 Operations Per Second (BOPS).

Intel microprocessor TeraScale Processor is designed under Tera-Scale Computing Research Program and is described in [3]. Terascale Processor integrates 80 cores in bi-dimensional mesh in 8 × 10 cores organization. With 65 nm processor technology implemented, chip integrates 100 million transistors on 275 mm^2 die. Processor performs 4 FLOP per cycle per core, and with 4.27 GHz delivers theoretical peak performance of 1.37 TFLOPS in single precision. Instructions set architecture consists of 16 instructions and Terascale Processor uses 96 bit VLIW. Each core runs own program and interconnection network transfers data and coordination instructions for execution of programs between cores via message passing.

Representative of DSP microprocessors with tile organization is VGI. Organization of 64 cores is 8 × 8 in bi-dimensional mesh and each core contains approximately 30 000 transistors. VGI utilizes dataflow paradigm of computation.

Whereas described architectures are integrating tens of cores, new approach to microprocessor design represented by spatial computing, with TRIPS, RAW, SmartMemories, nanoFabrics or WaveScalar representatives, is heading towards integration of hundreds or even thousands of simple cores or processing elements (PE) on the chip, often arranged along with memory elements in the grid [4][5][6][7].

3. DATA FLOW COMPUTING

Dataflow paradigm of computation was popularized in 60' and 70' and describes non Von Neumann architectures with the ability of fine grain parallelism in computation process.

In dataflow architecture the flow of computation is not instructions flood driven. There is no concept of program counter implemented in this architecture. Control of computation is realized by data flood. Instruction is executed immediately in condition there are all operands of this instruction present. When executed, instruction produces output operands, which are input operands for other instructions.

Dataflow paradigm of computing is using directed graph G = (V, E), called DataFlow Graph (DFG). DFG is used for the description of behaviour of data driven computer. Vertex v ∈ V is an actor, a directed edge e ∈ E describes precedence relationships of source actor to target actor and is guarantee of proper execution of the dataflow program. This assures proper order of instructions execution with contemporaneous parallel execution of instructions. Tokens are used to indicate presence of data in DFG.

Actor in dataflow program can be executed only in case there is a presence of a requisite number of data values (tokens) on input edges of an actor. When firing an actor execution, the defined number of tokens from input edges is consumed and defined number of tokens is produced to the output edges.

An important characteristic of dataflow program is its ability to detect parallelism of computation. This detection is allowed on the lowermost basis – on the machine instructions level.

There are static, dynamic and also hybrid dataflow computing models.

In static model, there is possibility to place only one token on the edge at the same time. When firing an actor, no token is allowed on the output edge of an actor. Disadvantage of the static model is impossibility to use dynamic forms of parallelism, such a loops and recursive parallelism. Computer with static dataflow architecture was designed by Denis and Misunas.

Dynamic model of dataflow computer architecture allows placing of more than one token on the edge at the same time. To allow implementation of this feature of the architecture, the tagging of tokens was established. Each token is tagged and the tag identifies conceptual position of token in the token flood.

For firing an actor execution, a condition must be fulfilled that on each input edge of an actor the token with the same tag must be identified. After firing of an actor, those tokens are consumed and predefined amount of tokens is produced to the output edges of an actor. There is no condition for firing an actor that no tokens must be placed on output edge of an actor.

The architecture of dynamic dataflow computer was first introduced at Massachusetts Institute of technology (MIT) as a Tagged Token Dataflow Architecture.

Hybrid dataflow architecture is a combination of control flow and data flow computation control mechanisms.

Dataflow computing is predominantly domain of the research laboratories and scientific institutions, and has limited impact on commercial computing because of difficulties in cost of communication, organization of computation, manipulation with structured data and cost of matching [8] [9] .

Paradigm of tile computing in combination with dataflow computing brings new possibilities to overcome some of deficiencies of dataflow architectures.

4. PROPOSED ARCHITECTURE

Proposed architecture is representative of computer-on-a-chip approach, which combines paradigm of computing with data driven computation model with principles of tile computing.

Architecture consists of elements with simple design, represented by processing elements (PE) and Input/Output elements (IO) and also comprises of interconnection network spread across the chip.

Processing elements are arranged in accordance with tile computing paradigm into bi-directional mesh of 8 × 8 PEs across the whole chip and processing elements are forming processing array (PA). Each PE integrates activation frames store as the storage of activation frames, arithmetic and logic unit for instructions execution and control unit. All PEs are unified general purpose computing units with simple design.

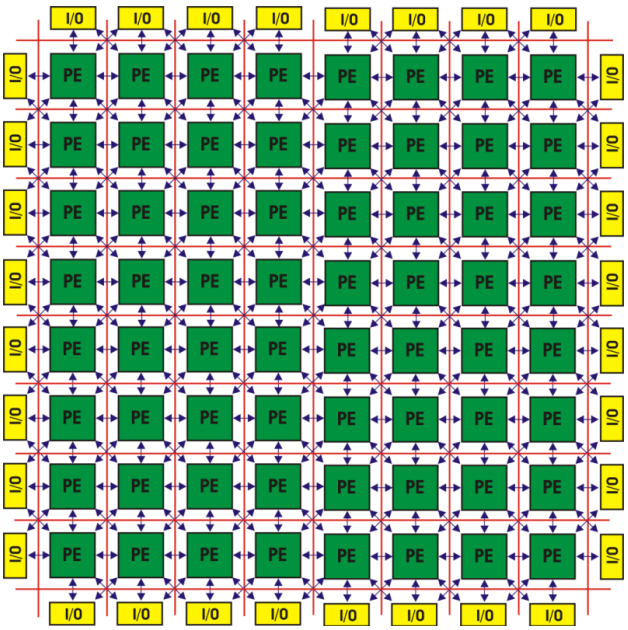

Fig. 1 Computer architecture with bi-directional mesh of processing elements in processing array (PA) with Input/Output elements on the edges of PA, local and global communication networks

Input and Output (IO) elements connected to the pins of the chip are localized at the edges of processing array. IOs are used not only for communication with surrounding equipment of computer, but also allow creation of multi-chip computer architectures, when IOs on different chips are creating bridges between PEs of different processing arrays.

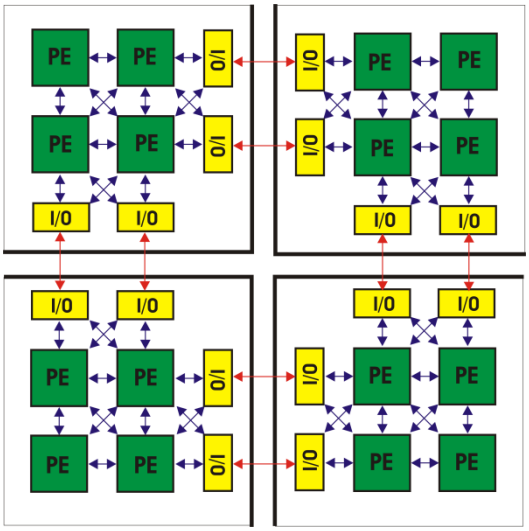

Fig. 2 Multichip configuration of computer

Interconnecting network allows concurrent short range high-bandwidth communication between pairs of neighbouring processing elements and also between processing elements and input/output elements. In this communication network processing element communicates directly with one of eight neighbours and allows speed communication over short distance.

Processing elements at the edges of the processing elements are able to communicate with I/O elements.

Global communication network allows data flow graph (DFG) mapping onto each activation frame of processing element in the processing array.

There are three modes of dataflow graph mapping, which allows not only sequential mapping of instructions into activation frames, but also allows concurrent mapping of instructions into activation frames stores of all processing elements of the array. This is called global mapping mode. There is also possibility of concurrent mapping of instructions into activation frames stores of selected processing elements of processing array. Selection of processing elements is allowed by use of mask. This is called mask mapping mode.

Advantages of proposed architecture with tile organization are in simple design of elements which are arranged across the chip in uniform simple manner which secures high-level scalability of the architecture. Decentralization of data storing, execution and control of computation results in shorter wire lengths on the chip and small latency in communication.

5. PROTOTYPE

Prototype of dataflow computer with proposed architecture is realized with software development software tool ISE WebPack for architecture development and a software tool ModelSim for simulation and verification of function of realized design.

Simulation is oriented to Spartan 3 FPGA chip and hardware prototype of the computer is built-up with use of Xilinx Spartan 3 PCIe Starter board as the hardware platform of the prototype. There is an FPGA chip Xilinx Spartan 3 XC3S1000-4FG676 with 676 pins in FBGA package in the centre of development board and it works on 50 MHz clock frequency. There are 391 free for use pins in this chip and 17000 logic cells.

Development board involves 4 Mb serial flash memory. There are 8 light emitting diodes (LED) for diagnostics and development purpose on the design board. There is also 9-pin RS 232 serial interface and 168 pins expansion ports which functions are configurable in accordance with the design on the board.

Fig. 3 Spartan 3AN Development Board

6. CONCLUSIONS

Contribution of this work is in the design of the architecture and realization of software simulation of dataflow computer with the tile based architecture, which allows further research in the field oriented on possibilities of utilization of dataflow computing in praxis and brings possibilities to overcome some disadvantages of dataflow paradigm.

In the future research evaluation of possibility to use this architecture for construction of high throughput active elements of networks will take place.

This work introduced paradigm of tile based computing, dataflow computing and introduced details of dataflow computer architecture designed at the Department of Computers and Informatics, Faculty of Electrical Engineering and Informatics at Technical University of Košice.

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REFERENCES

[1] WAINGOLD, E. – TAYLOR, M. – SRIKRISHNA, D. – SARKAR, V. – LEE, W. – LEE, V. – KIM, J. – FRANK, M. – FINCH, P. – BARUA, R. – BABB, J. – AMARASINGHE, S. – AGARWAL, A.: Baring it all to software: RAW machines. IEEE Computer, 30(9):86–93, September 1997, Technical Report, Massachusetts Institute of Technology Cambridge, MA, USA.

[2] WINTZLAW, D. – GRIFFIN P. – HOFFMANN, H. – BAO, L. – EDWARDS, B. – RAMEY, C. – MATTINA, M. – MIAO, CH. – BROWN III, J. F. – AGARWAL, A.: On-Chip Interconnection Architecture of the Tile Processor, IEEE Micro, vol. 27, no. 5, pp. 15–31, Sep./Oct. 2007, doi:10.1109/MM. 2007.89.

[3] MATTSON, T. G. – VAN DER WIJNGAART, R. – FRUMKIN, M.: Programming the Intel 80-core network-on-a-chip Terascale Processor, SC2008 November 2008, Austin, Texas, USA 978-1-4244-2835-9/08.

[4] MERCALDI, M. – SWANSON, S. – PETERSEN, A. – PUTNAM, A. – SCHWERIN, A. – OSKIN, M. – EGGERS, J. S.: Modelling Instruction Placement on a Spatial Architecture, SPAA'06, July 30 – August 2, 2006, Cambridge, Massachusetts, USA 1-59593-452-9/06/0007 ACM.

[5] MAI, K. – PAASKE, T. – NUWAN, J. – HO, R. – DALLY, W. – HOROWITZ, M.: Smart Memories: A Modular Reconfigurable Architecture, ISCA 00, Vancouver, British Columbia, Canada, ACM 1-58113-287-5/00/06-161.

[6] SAKARALINGAM, R. – NAGARAJAN, R. – MCDONALD, R. – DESIKAN, S. – DROLICA, S. – GOVIDAN, S. – GRATZ, P. – GULATI, D. – HANSON, H. – KIM, CH. – LIU, H. – RANGANATHAN, N. – SETHUMADHAVAN, S. – SHARIF, S. – SHIVAKUMAR, P. – KECKLER, S. W. – BURGER, D.: Distributed Microarchitectural Protools in the STRIP Prototype Processor, The 39th Annual IEEE/ACM International Symposium on Microarchitecture (MICRO'06) 0-7695-2732-9/06.

[7] BUDIU, M. – VENKATARAMANI, T. – CHELCEA, T. – GOLDSTEIN, S. C.: Spatial Computation, In International Conference on Architectural Support for Programming Languages and Operating Systems, pp. 14–26, October 2004.

[8] VOKOROKOS, L. – ÁDÁM, N.: Operators Matching in Dynamic Data Flow Architectures, Conference on Computation Cybernetics, Vienna, Austria, August 30 – September 1, Vienna, 2004, pp. 77–81, ISBN 3-902463-02-3.

[9] VOKOROKOS, L. – ÁDÁM, N. – BALÁŽ, A.: Flexible Platform for Neural Network Based on Data Flow Principles, HUCI, Budapest, November 18–19, Budapest Tech, 2005.

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