SIMPLE AND NOVEL UNIFIED PULSE WIDTH MODULATION ALGORITHM FOR VOLTAGE SOURCE INVERTERS IN THE ENTIRE MODULATION RANGE

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ABSTRACT

This paper presents a simple and novel carrier based unified pulse width modulation (UPWM) algorithm for voltage source inverter (VSI) fed AC drives. To reduce the complexity involved in the existing PWM algorithms due to angle and sector information, the proposed UPWM algorithm uses the notion of imaginary switching times, which uses the instantaneous phase voltages only. To validate the proposed algorithm at all modulation indices, a simple over modulation algorithm is also presented in this paper. By varying the offset time in the proposed UPWM algorithm various continuous PWM (CPWM) algorithms like sinusoidal PWM (SPWM) and space vector PWM (SVPWM) and discontinuous PWM (DPWM) algorithms such as DPWMMIN, DPWMMAX, DPWM0, DPWM1, DPWM2 and DPWM3 can be generated at all modulation indices. To verify the proposed UPWM algorithm, numerical simulation studies have been carried out and results are presented.

Keywords: *Discontinuous PWM, PWM, SVPWM, VSI*

1. INTRODUCTION

Due to the inventions of fast switching power semiconductor devices and motor control algorithms, a growing interest is found in a more precise pulse width modulation (PWM) method. During the past decades several PWM algorithms have been studied extensively. Various PWM methods have been developed to achieve wide linear modulation range, less switching loss, less total harmonic distortion (THD), easy implementation and less computation time. A large variety number of PWM algorithms exist and a survey of these was given by Holtz [1]. There are two popular approaches for the implementation of PWM algorithms, namely triangular comparison (TC) approach and space vector (SV) approach. For the implementation point of view, TC approach is simple when compared to SV approach. However, the SV approach provides more degrees of freedom in the implementation when compared to TC approach as explained in [2]. The earliest modulation signals for TC approach based PWM are sinusoidal. But, the addition of the zero sequence signals to the sinusoidal signals results in several non-sinusoidal signals. Compared with sinusoidal PWM (SPWM) algorithm, non-sinusoidal PWM algorithms can extend the linear modulation range for line-to-line voltages. Different zero-sequence signals lead to different non sinusoidal PWM modulators.

Nowadays, due to the development of digital signal processors, SVPWM has become one of the most popular PWM methods for three-phase inverters [3]. It uses the SV approach to compute the duty cycle of the switches. The main features of this PWM algorithm are easy digital implementation and wide linear modulation range for output line-to-line voltages. Though, the SVPWM gives superior performance, it gives more switching losses of the inverter as it has continuous modulating signal. Hence, to reduce the switching losses of the inverter, nowadays discontinuous PWM (DPWM) algorithms are becoming popular. The generation of these DPWM algorithms is given in detail in the literature [4]-[9]. However, the conventional space vector approach requires angle and sector information and hence increases the complexity involved in the algorithm. To reduce the complexity involved, a simplified approach has been proposed in [5] by using the concept of magnitude test. A simple generalized PWM algorithm has been proposed in [8] by using the concept of offset voltage under the linear modulation region. A simple approach has been proposed in [7], [9] by using the concept of imaginary switching times. Moreover, over modulation is of a remarkable importance, especially in the variable speed drives an application where it is necessary to reach the maximum motor torque. A good over modulation strategy should manage the transition from PWM to six-step control avoiding the abrupt voltage changes to the motor.

This paper presents a novel and simple UPWM algorithm, which is developed by using the concept of imaginary switching times. In the proposed UPWM algorithm, generalized expression for offset time is derived and then by varying the offset time various PWM algorithms can be generated at all modulation indices.

2. CONVENTIONAL SVPWM ALGORITHM

The main purpose of the voltage source inverter (VSI) is to generate a three-phase voltage with controllable amplitude, and frequency. A general 2-level, 3-phase VSI feeding a three-phase induction motor is shown in Fig 1. From Fig. 1, it can be observed that the two switching devices on the same leg cannot be turned on and cannot be turned off at the same time, which will result in the uncertain voltage to the connected phase. Thus the nature of the two switches on the same leg is complementary. The switching-on and switching-off sequences of a switching device are represented by an existence function, which has a value of unity when it is turned on and becomes zero when it is turned off. The existence function

of a VSI comprising of switching devices T_i is represented by S_i, $i = 1, 2, \ldots, 6$. Hence, S_1, S_4 which take values of zero or unity respectively, are the existence functions of the top device (T_1) and bottom device (T_4) of the inverter leg which is connected to phase 'a'.

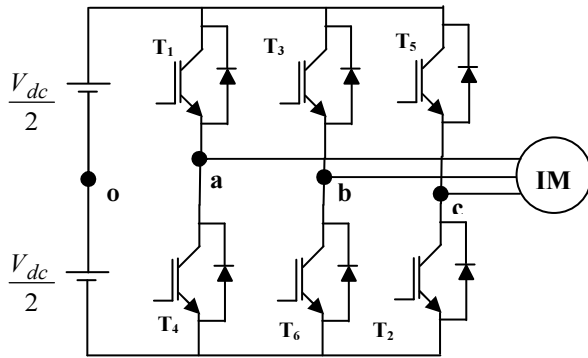$$S_1 + S_4 = 1; \ S_3 + S_6 = 1; \ S_5 + S_2 = 1 \tag{1}$$

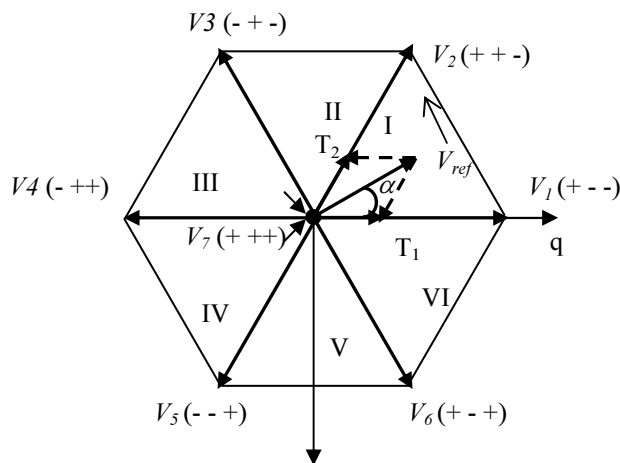**Fig. 1** Two-level, 3-phase voltage source inverter feeding induction motor

Fig. 2 Voltage space vectors produced by a voltage source inverter

As seen from Fig 1, there are totally six switching devices and only three of them are independent. The combination of these three switching states gives out eight possible voltage vectors. At any time, the inverter has to operate one of these voltage vectors. Out of eight voltage vectors, two are zero voltage vectors (V_0 and V_7) and remaining six (V_1 to V_6) are active voltage vectors. Hence, the possible eight different switching states of the three-phase inverter can be represented in the space vector plane as shown in Fig. 2.

For a given set of inverter phase voltages (V_{an}, V_{bn}, V_{cn}), the space vector can be constructed as

$$V_s = \frac{2}{3}\left(V_{an} + V_{bn}e^{j\frac{2\pi}{3}} + V_{cn}e^{j\frac{4\pi}{3}} \right) \tag{2}$$

From (2), it is easily shown that the active voltage vectors or active states can be represented as

$$V_k = \frac{2}{3}V_{dc}e^{j(k-1)\frac{\pi}{3}} \tag{3}$$

where $k = 1, 2, \ldots, 6$

By maintaining the volt-second balance, a combination of switching states can be utilized to generate a given sample in an average sense during a subcycle. The voltage vector V_{ref} in Fig. 2 represents the reference voltage space vector or sample, corresponding to the desired value of the fundamental components for the output phase voltages. But, there is no direct way to generate the sample and hence the sample can be reproduced in the average sense. The reference vector is sampled at equal intervals of time, T_s referred to as sampling time period. Different voltage vectors that can be produced by the inverter are applied over different durations with in a sampling time period such that the average vector produced over the subcycle is equal to the sampled value of the reference vector, both in terms of magnitude and angle. As all the six sectors are symmetrical, here the discussion is limited to sector-I only.

Let T_1 and T_2 be the durations for which the active states 1 and 2 are to be applied respectively in a given sampling time period T_s. Let T_z be the total duration for which the zero states are to be applied. From the principle of volt-time balance T_1, T_2 and T_z can be calculated as

$$T_1 = \frac{2\sqrt{3}}{\pi}M\left[Sin(60^o - \alpha)\right]T_s \tag{4}$$

$$T_2 = \frac{2\sqrt{3}}{\pi}M\left[Sin(\alpha)\right]T_s \tag{5}$$

$$T_Z = T_s - T_1 - T_2 \tag{6}$$

where M is known as the modulation index and given

as $M = \dfrac{\pi V_{\text{ref}}}{V_{dc}}$.

In the SVPWM algorithm, the maximum modulation index is 0.906. In the SVPWM strategy, the total zero voltage vector time is equally distributed between V_0 and V_7. Further, in this method, the zero voltage vector time is distributed symmetrically at the start and end of the subcycle in a symmetrical manner. Moreover, to minimize the switching frequency of the inverter, it is desirable that switching should take place in one phase of the inverter only for a transition from one state to another. Thus, SVPWM uses 0127-7210 in first sector, 0327-7230 in second sector and so on. Also, with the SVPWM algorithm, the modulation index and dc bus utilization can be increased when compared with the SPWM algorithm.

3. PROPOSED UPWM ALGORITHM

Instead of equal distribution of zero voltage vector time among the two possible zero voltage vectors, the proposed UPWM algorithm uses unequal distribution of zero state time. By varying the zero voltage vector time variation as $T_0 = \mu T_z$ and $T_7 = (1-\mu)T_z$, various discontinuous PWM (DPWM) algorithms can be developed. Where, μ varies between 0 and 1. Since all of these different schemes are based on the division of zero voltage vector time, it is possible to derive the general expression that is used to generate all the possibilities. Thus, to generate the various DPWM methods along with the SPWM and SVPWM algorithms, the proposed algorithm has been proposed. Moreover, to reduce the complexity involved in conventional SVPWM algorithm, the proposed PWM algorithm uses reference phase voltages.

The time durations of the active voltage vectors can be represented in terms of phase voltages or line to line voltages as given in (7) – (8) [7].

$$T_1 = \frac{T_s}{V_{dc}}V_{an} - \frac{T_s}{V_{dc}}V_{bn} \equiv \frac{T_s}{V_{dc}}(V_{an} - V_{bn}) \equiv T_s \frac{V_{ab}}{V_{dc}} \quad (7)$$

$$T_2 = \frac{T_s}{V_{dc}}V_{bn} - \frac{T_s}{V_{dc}}V_{cn} \equiv \frac{T_s}{V_{dc}}(V_{bn} - V_{cn}) \equiv T_s \frac{V_{bc}}{V_{dc}} \quad (8)$$

The switching times in each sector in terms of line voltages and maximum and minimum voltages in each sector are given in Table 1. Also, in a balanced three-phase system as shown in Fig 1, the sum of the three phase voltages is zero. Then the voltage between neutral of the induction motor and reference point of the DC source, which is also known as common mode voltage or neutral voltage, is determined from (9).

$$V_{no} = \frac{V_{dc}}{3}\left(S_1 + S_3 + S_5 - \frac{3}{2}\right) \quad (9)$$

Table 1 Device switching times expressed in terms of reference line-line voltages

	Sector-I	Sector-II	Sector-III	Sector-IV	Sector-V	Sector-VI
V_{max}	V_{an}	V_{bn}	V_{bn}	V_{cn}	V_{cn}	V_{an}
V_{min}	V_{cn}	V_{cn}	V_{an}	V_{an}	V_{bn}	V_{bn}
T_1	$T_s\frac{V_{ab}}{V_{dc}}$	$T_s\frac{V_{ba}}{V_{dc}}$	$T_s\frac{V_{bc}}{V_{dc}}$	$T_s\frac{V_{cb}}{V_{dc}}$	$T_s\frac{V_{ca}}{V_{dc}}$	$T_s\frac{V_{ac}}{V_{dc}}$
T_2	$T_s\frac{V_{bc}}{V_{dc}}$	$T_s\frac{V_{ac}}{V_{dc}}$	$T_s\frac{V_{ca}}{V_{dc}}$	$T_s\frac{V_{ba}}{V_{dc}}$	$T_s\frac{V_{ab}}{V_{dc}}$	$T_s\frac{V_{cb}}{V_{dc}}$

where V_{max} and V_{min} represents maximum and minimum phase voltages in every sampling interval.

The general expression for the average neutral voltage, V_{no}, can be determined using the method of space vector modulation and the voltages of the three-phase voltage source converter. For example, in first sector $V_{max} = V_a$, $V_{min} = V_c$. For a balanced three-phase supply system, $V_b = -(V_{max} + V_{min})$. Hence, the switching times can be rewritten as (10).

$$T_1 = \frac{2V_{max} + V_{min}}{V_{dc}}T_s; \quad T_2 = \frac{-V_{max} - 2V_{min}}{V_{dc}}T_s;$$

$$T_z = \left(1 - \frac{V_{max} - V_{min}}{V_{dc}}\right)T_s \quad (10)$$

The average neutral voltage is

$$V_{no} = \frac{1}{T_s}\left(V_{no1}T_1 + V_{no2}T_2 + V_{no0}T_0 + V_{no7}T_7\right) =$$

$$= \frac{V_{dc}}{6}\left(\frac{T_2 - T_1}{T_s}\right) + \frac{V_{dc}}{2}(1-2\mu)\left(\frac{T_z}{T_s}\right) \quad (11)$$

By substituting (10) in (11), the expression for neutral voltage can be obtained as

$$V_{no} = \frac{V_{dc}}{2}(1-2\mu) + (\mu-1)V_{max} - \mu V_{min} \quad (12)$$

Hence, the modulating voltage waveforms can be represented as given (13).

$$V_{in}^* = V_{in} + V_{no} \qquad i = a,b,c \quad (13)$$

The actual gating times can be calculated by using the concept of imaginary switching times. The value of imaginary switching time is directly related to the phase voltage and can be expresses as given in (14).

$$T_{an} = \frac{V_{an}}{V_{dc}}T_s; \quad T_{bn} = \frac{V_{bn}}{V_{dc}}T_s; \quad T_{cn} = \frac{V_{cn}}{V_{dc}}T_s \quad (14)$$

These switching times could be negative when the phase voltage is negative and hence these are called as imaginary switching times. The maximum and minimum imaginary switching times can be evaluated in each sampling interval from (15).

$$T_{max} = max(T_{an}, T_{bn}, T_{cn}); \quad T_{min} = min(T_{an}, T_{bn}, T_{cn}) \quad (15)$$

Then the general relation between the actual gating times and the modulating voltage waveforms is as given in (16).

$$T_{gi} = \frac{T_s}{2}\left(1 + \frac{2V_{in}^*}{V_{dc}}\right) \quad (16)$$

By substituting (12) and (13) in (16), the general expression for actual gating times can be obtained as

$$T_{gi} = T_{in} + T_{offset} \quad (17)$$

where

$$T_{offset} = T_s(1-\mu) + (\mu-1)T_{max} - \mu T_{min} \quad \text{for SVPWM and DPWM}$$

$$T_{offset} = T_s/2 \qquad \text{for SPWM} \quad (18)$$

In the implementation of the proposed offset time based unified PWM algorithm, the zero voltage vector time partition parameter (μ) can take any form (constant or time-varying) ranging between 0 and 1. The choice of μ affects the average neutral voltage. In the conventional

SVPWM algorithm, as the zero voltage vector time is distributed equally, μ is generally taken as 0.5. If μ is either 0 or 1, each switching device ceases to switch for a total of 120 degrees per fundamental cycle. Hence, the switching losses and effective inverter switching frequency are significantly reduced. As the modulating signals are discontinuous, these PWM algorithms are also known as DPWM algorithms or bus-clamping PWM algorithms. The selection of μ gives rise to an infinite number of possible PWM algorithms, some of which have been referred in [7]-[8]. To obtain the various DPWM algorithms, μ is taken as given (19).

$$\mu = 1 - 0.5\big[1 + \mathrm{sgn}\big(\cos 3(\omega t + \delta)\big)\big] \qquad (19)$$

where sgn(X) is 1, 0 and –1 when X is positive, zero, and negative, respectively. By varying the modulation angle δ, various DPWM algorithms are generated. The SVPWM, DPWMMIN and DPWMMAX algorithms can be obtained for μ = 0.5, 1 and 0 respectively. Moreover, DPWM0, DPWM1, DPWM2 and DPWM3 can be obtained for δ = π/6, 0, - π/6 and - π/3 respectively. Finally, the expression for the modulating waveform of unified PWM algorithm can be given as

$$V_{in}^* = \frac{V_{dc}}{2}\left(\frac{2 * T_{gi}}{T_s} - 1\right) \qquad (20)$$

The generated modulating waveforms and reference phase voltage of various PWM algorithms at a modulation index of 0.7 are shown in Fig. 3.
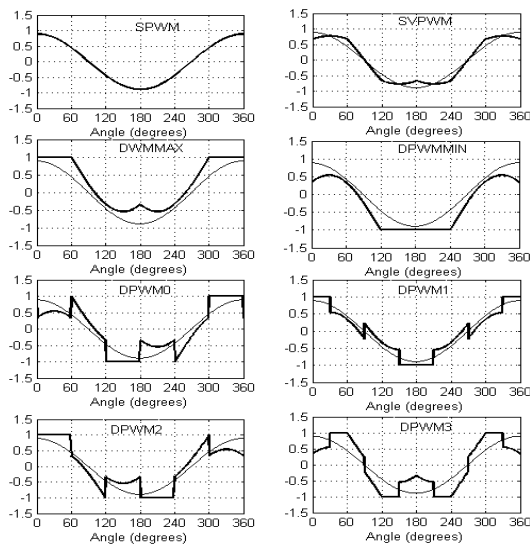
Fig. 3 Modulating waveforms of various PWM algorithms at a modulation index of 0.7

4. PROPOSED UPWM ALGORITHM IN THE OVER MODULATION REGION

As the maximum magnitude of the inverter output voltage is limited by V_{dc}, in order to guarantee the linearity of the inverter output voltage, the reference vector should reside in the hexagon region. However, in the transient state of the drive system V_{ref} may exceed the hexagon area, as shown in Fig 4. In this case, the effective time, which is the sum of the two active voltage vector times ($T_1 + T_2$) becomes larger than the sampling time. A proper over modulation technique should be implemented, because it determines the transient dynamics of the system. In the proposed UPWM scheme, a commonly used simple over modulation strategy is used, in which the available voltage vector at point "b" is selected instead of the original reference vector at point "a" as shown in Fig .4. The offset time and the actual gating times can be simply calculated as follows:

$$T^1{}_{an,bn,cn} = T_{an,bn,cn} * \frac{T_s}{T_{eff}} \qquad (21)$$

$$T_{offset} = -T\min * \frac{T_s}{T_{eff}} \qquad (22)$$

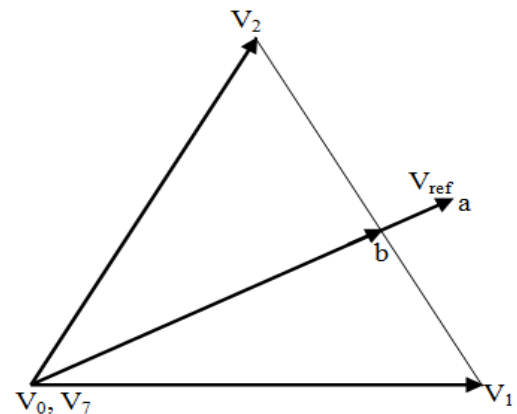$$T_{ga,gb,gc} = T^1{}_{an,bn,cn} + T_{offset} \qquad (23)$$

Fig. 4 Voltage vectors in the over modulation region.

5. SIMULATION RESULTS AND DISCUSSION

To validate the proposed PWM algorithms, several numerical simulation studies have been carried out using Matlab-Simulink. To maintain constant average switching frequency, the switching frequency of SVPWM algorithm is taken as f_s and DPWM algorithms is taken as $1.5 f_s$. Since, in the DPWM algorithms, the modulating wave is clamped for 120 degrees and hence these reduce the switching frequency by 33.33%.

For the simulation studies, the average switching frequency of the inverter is taken as 3 kHz and the dc link voltage is taken as 600V. The simulation studies are carried out for two different modulation indices one is at linear modulation range and another one is at over modulation range. The simulation results of various PWM algorithms are shown in from Fig. 5 to Fig. 18.
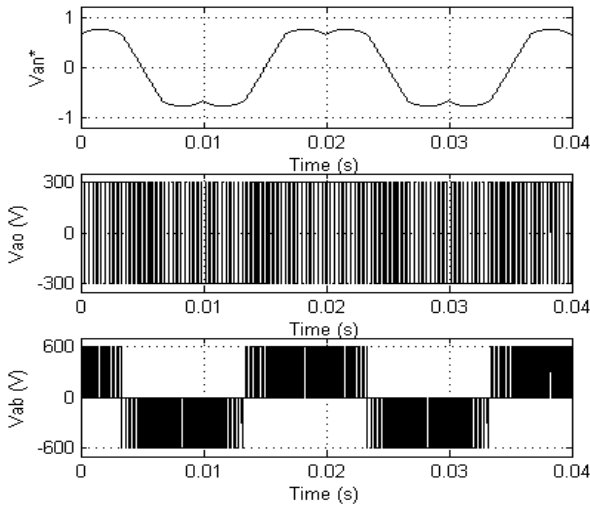
Fig. 5 Simulation results of SVPWM algorithm (modulating wave, pole voltage and line voltages) at M=0.7
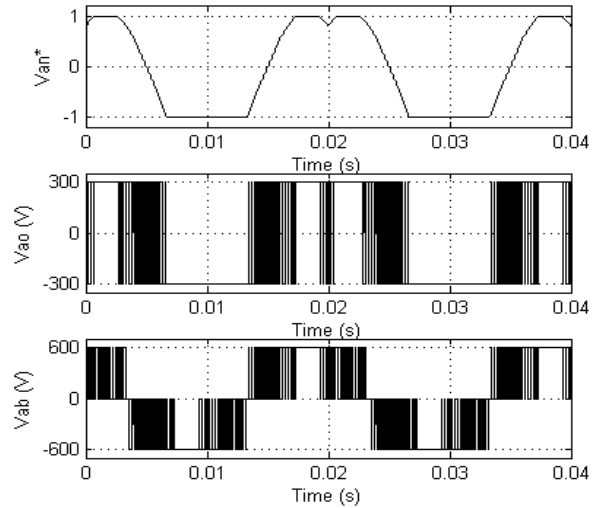

Fig. 8 Simulation results of DPWMMIN algorithm (modulating wave, pole voltage and line voltages) at M=0.95
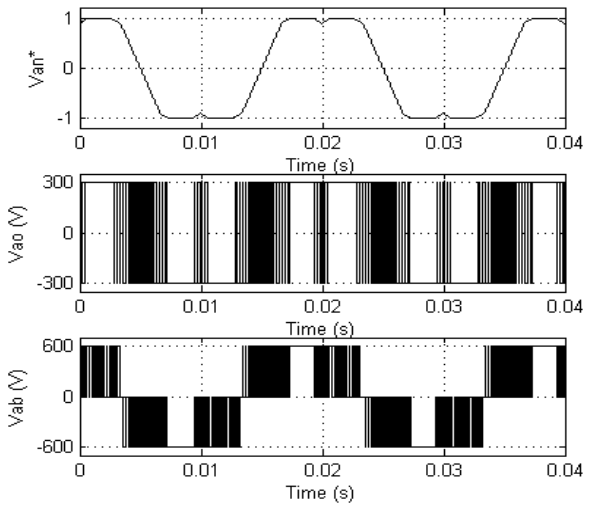

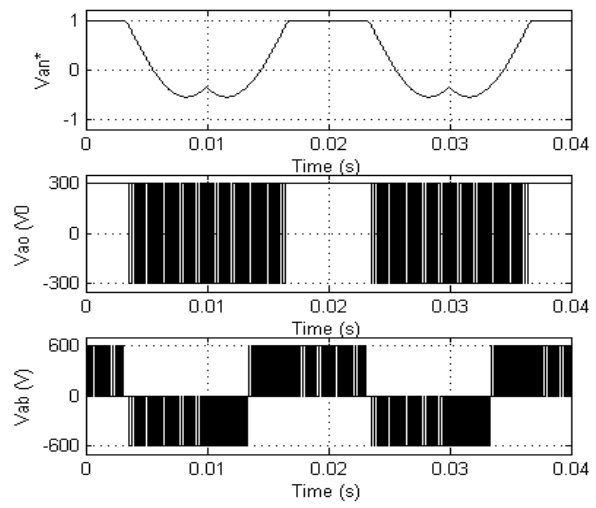**Fig. 6** Simulation results of SVPWM algorithm (modulating wave, pole voltage and line voltages) at M=0.95

Fig. 9 Simulation results of DPWMMAX algorithm (modulating wave, pole voltage and line voltages) at M=0.7
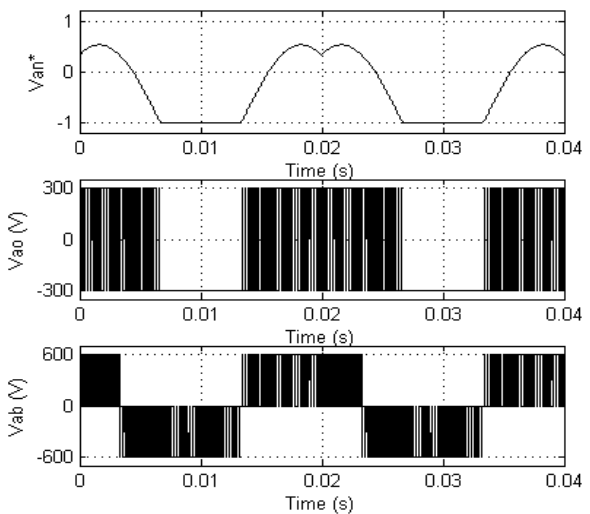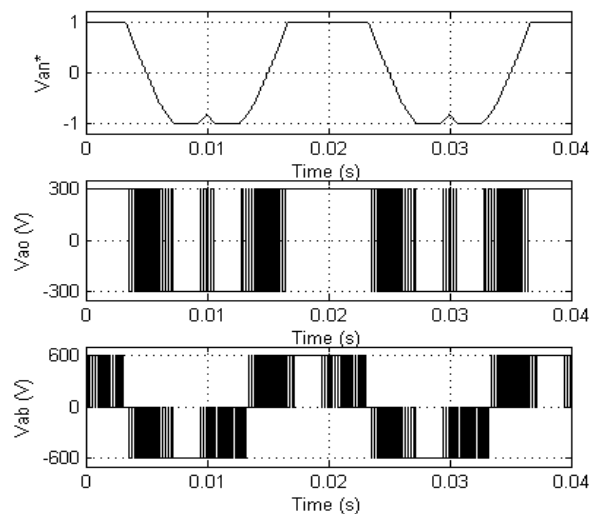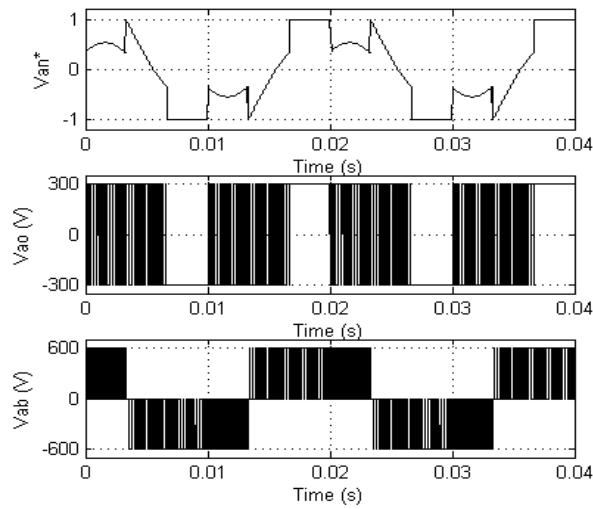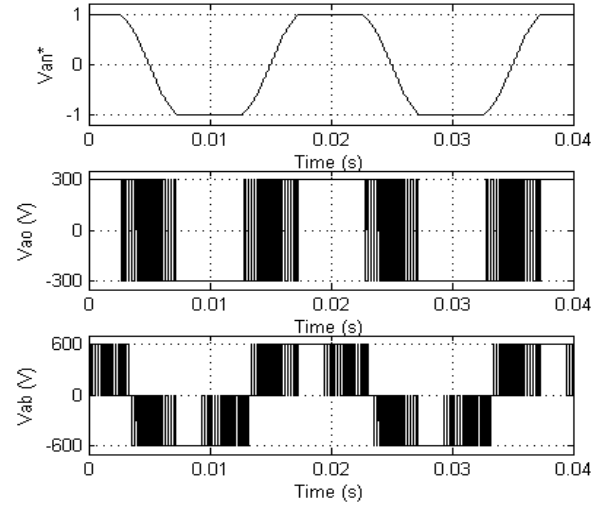

Fig. 7 Simulation results of DPWMMIN algorithm (modulating wave, pole voltage and line voltages) at M=0.7

Fig. 10 Simulation results of DPWMMAX algorithm (modulating wave, pole voltage and line voltages) at M=0.95

Fig. 11 Simulation results of DPWM0 algorithm (modulating wave, pole voltage and line voltages) at M=0.7

Fig. 14 Simulation results of DPWM1 algorithm (modulating wave, pole voltage and line voltages) at M=0.95
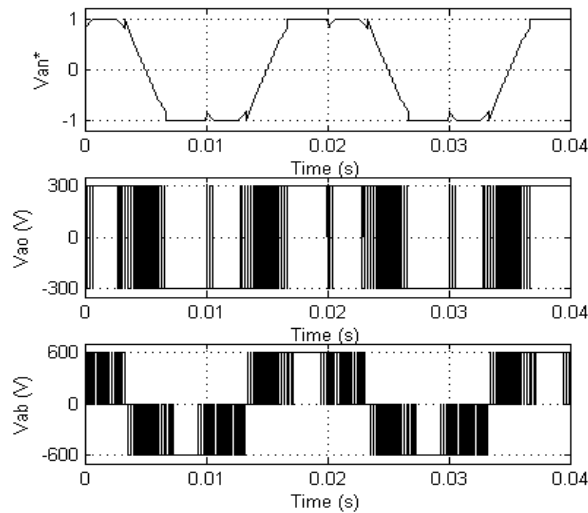

Fig. 12 Simulation results of DPWM0 algorithm (modulating wave, pole voltage and line voltages) at M=0.95
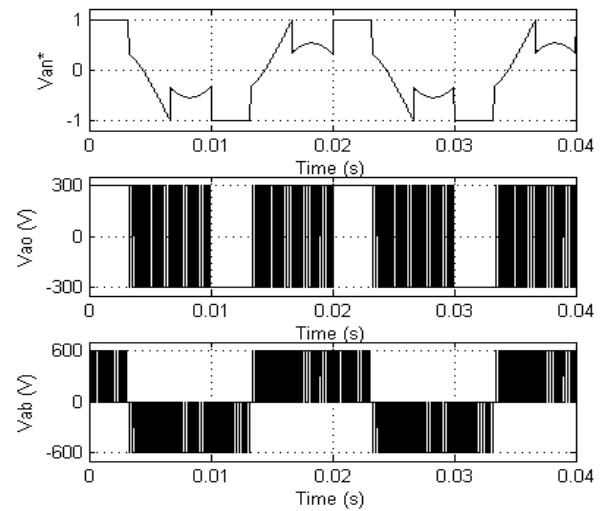

Fig. 15 Simulation results of DPWM2 algorithm (modulating wave, pole voltage and line voltages) at M=0.7
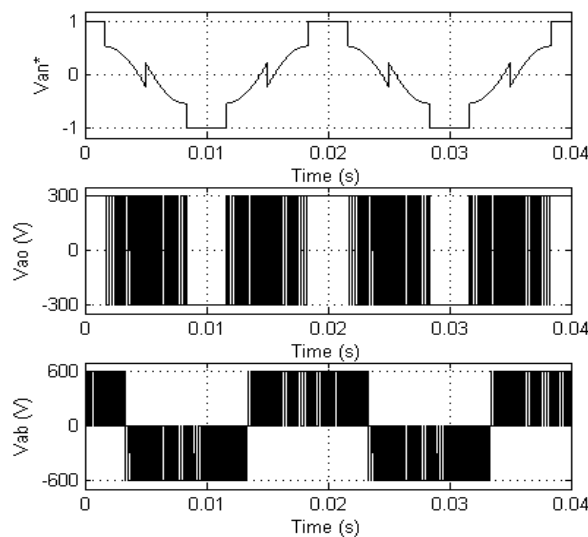

Fig. 13 Simulation results of DPWM1 algorithm (modulating wave, pole voltage and line voltages) at M=0.7
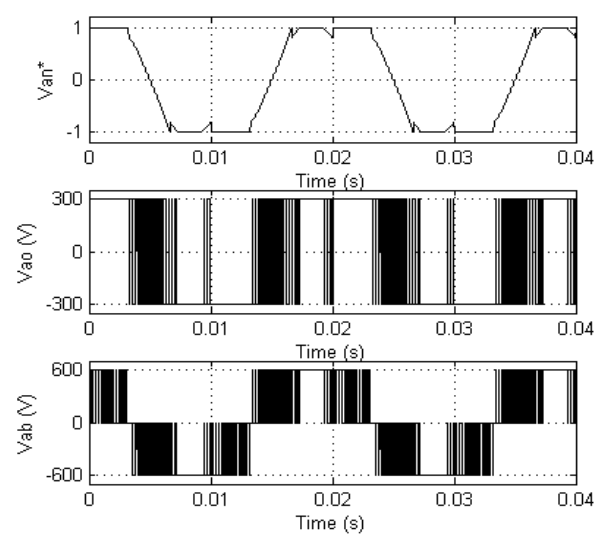

Fig. 16 Simulation results of DPWM2 algorithm (modulating wave, pole voltage and line voltages) at M=0.95
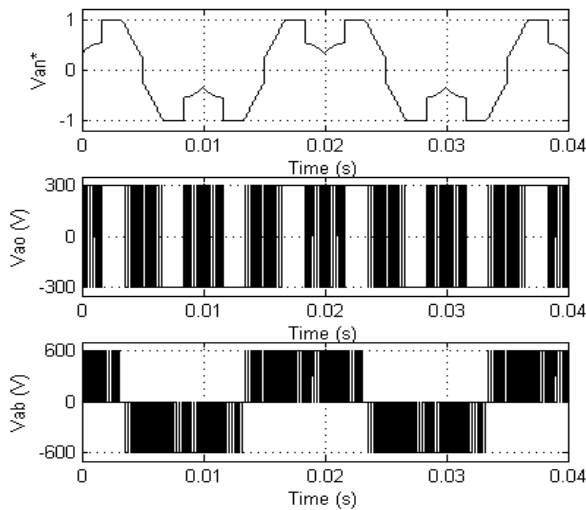
Fig. 17 Simulation results of DPWM3 algorithm (modulating wave, pole voltage and line voltages) at M=0.7
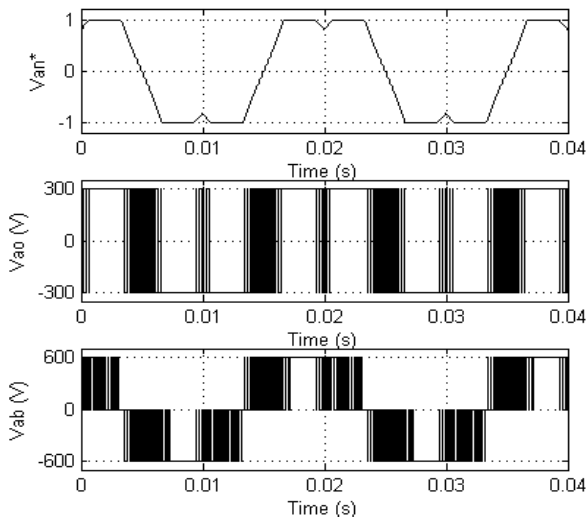

Fig. 18 Simulation results of DPWM3 algorithm (modulating wave, pole voltage and line voltages) at M=0.95

From the simulation results, it can be observed that as the SVPWM algorithm is a continuous PWM algorithm and hence it gives continuous pulse pattern and more switching losses. Whereas the DPWM algorithms clamp each phase to either positive DC bus or negative DC bus for 120 degrees over a fundamental cycle. Hence, the DPWM algorithms reduce the switching frequency and switching losses by 33.33% when compared with the continuous PWM algorithms. Thus, the proposed UPWM algorithm generates a wide range of PWM algorithms in the entire modulation range with reduced complexity by varying a parameter μ from 0 and 1.

6. CONCLUSIONS

A simple and novel unified PWM algorithm has been proposed in this paper. The proposed algorithm generates

a wide range of PWM algorithms which include both the continuous and discontinuous PWM algorithms. To validate the proposed UPWM algorithm, the simulation results have been presented. From the simulation results it can be observed that the proposed UPWM algorithm gives a wide range of PWM algorithms in the entire modulation range with reduced complexity on the existing algorithms. Moreover, from the simulation results it can be concluded that the DPWM algorithms ceases the pulses by 120 degrees in every fundamental cycle and hence reduce the switching losses of the inverter by 33.33 percent.

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BIOGRAPHIES

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