GENERALIZED PWM TECHNIQUE FOR DUAL INVERTER FED INDUCTION MOTOR DRIVE

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ABSTRACT

This paper presents a simplified Generalized Pulse Width Modulation (GPWM) algorithm to obtain various continuous and discontinuous PWM algorithms for a four-level inverter topology. The proposed four-level inverter is achieved by feeding the induction motor from both ends by a three-level cascade inverter from one side and by two-level inverter from other side. The proposed inverter configuration is capable to produce an output voltage of two-level, three-level and four-level in entire modulation range. In the proposed inverter topology neutral point fluctuations are absent and neutral clamping diodes are absent. With the application of various discontinuous PWM algorithms to the proposed inverter topology the switching losses are reduced when compared with continuous PWM algorithm. The simulation analyses are carried out in MATLAB/simulink environment and the results are presented.

Keywords: *Cascade inverter, GPWM, open end winding induction motor, SVPWM*

1. INTRODUCTION

Voltage Source Inverters (VSI) are getting popularized in adjustable speed drive applications. To control the output voltage and output frequency of VSI, the pulse width modulation (PWM) techniques are employed. The switching fashion employed in PWM techniques reduces harmonics in the output voltage. Based on switching fashion different PWM techniques are proposed in literature [1-5]. Among Various PWM techniques space vector pulse width modulation (SVPWM) technique proposed in [4-5] gives superior performance for a voltage source inverter. SVPWM discussed in [4], in a given sampling time (T_s) the switching times for which active voltage vectors and zero voltage vectors times are given by (1). In conventional SVPWM algorithm, the zero vector time (T_z) is divided equally among the two possible zero states. The calculation of switching times (T_1, T_2, T_z) require angular information (α) and magnitude of reference voltage (V_{ref}) at each instant, which makes the SVPWM algorithm complex.

$$\begin{aligned} T_1 &= \frac{2\sqrt{3}}{\pi} M_i \sin\left(60^0 - \alpha\right) T_s \\ T_2 &= \frac{2\sqrt{3}}{\pi} M_i \sin(\alpha) T_s \\ T_Z &= T_s - T_1 - T_2 \end{aligned} \tag{1}$$

where M_i is the modulation index $M_i = \frac{\pi V_{ref}}{2V_{dc}}$.

In [5], the authors proposed a simplified algorithm where no need to calculate the angular information by using the concept of imaginary switching times. Along with simplification of algorithm, various discontinuous PWM algorithms have been presented in [7-8] by unequal division of zero state times.

However, the two-level inverters produce more harmonic distortion. In two-level inverter topologies as switching frequency increases the harmonic content in line current gets reduced. In order to have low harmonic content at low switching frequency multilevel inverter topologies are employed. Different multilevel inverter topologies are presented in literature [9-10]. Conventional Multilevel inverter topologies like diode clamped and H-bridge topologies discussed in [9-11] require clamping diodes, separate DC-link voltages sources for their operation. Multilevel inverter topologies have the drawbacks of neutral point fluctuations and complexity increases as number of levels increases. To overcome these drawbacks and reduce complexity cascade and dual inverter topologies are presented in literature. As multilevel inverter topologies can synthesis output voltage waveform from small individual voltage sources. Two two-level inverters are cascaded to generated three level output voltage, this configuration is called cascade inverter topology proposed in literature [12]. Similarly two two-level inverter topologies feed the load from both ends called dual inverter configuration is proposed in literature [13]. Both cascade and dual inverter topologies are combined as shown in Fig.1 to generate four-level output voltage [14-15].

In this paper, a simplified and more generalized approach is presented to generate all possible continuous and discontinuous PWM (DPWM) signals by adding a zero sequence voltage to the commanded reference signals. The harmonic content in the output voltage is low at low switching frequency by employing proposed topology. But the switching losses can also be reduced by employing various DPWM algorithms.

2. PROPOSED INVERTER TOPOLOGY

The proposed circuit topology is obtained by feeding induction motor from both ends by three-level cascade inverter and two-level inverter as shown in Fig. 1.

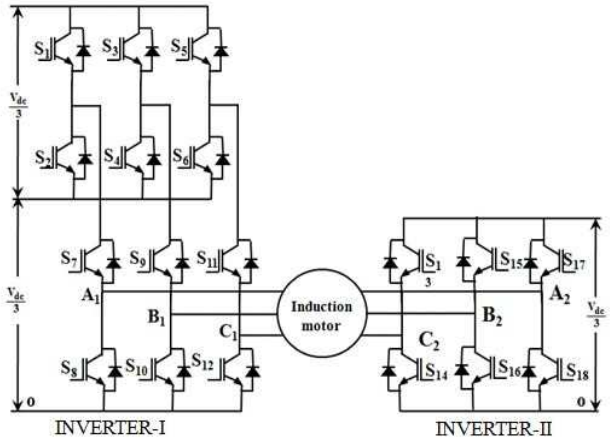

Fig. 1 Proposed inverter topology

V_{A1o},V_{B1o},V_{C1o} represents the pole voltage of inverter-I. As two inverters are cascaded inverter-I can generate three level output voltage.$V_{A2o'}$, $V_{B2o'}$, $V_{C2o'}$ are the pole voltages of Inverter-II. V_{A1A2}, V_{B1B2}, V_{C1C2} are the effective phase voltages. The combined pole voltage of proposed multi level inverter are given by

$$\begin{aligned} V_A &= V_{A1O} - V_{A2O} \\ V_B &= V_{B1O} - V_{B2O} \\ V_C &= V_{C1O} - V_{C2O} \end{aligned} \tag{2}$$

To control the output voltage and frequency of proposed inverter topology, various carrier based PWM algorithms are presented in this paper. In multilevel inverter topologies to generate N-level output voltage (N-1) level shifting triangles are required. So for the proposed topology, to generate four-level output, three level shifting triangles are required. The level shifting triangles are divided into three regions R1, R2 and R3 as shown in Fig. 2.

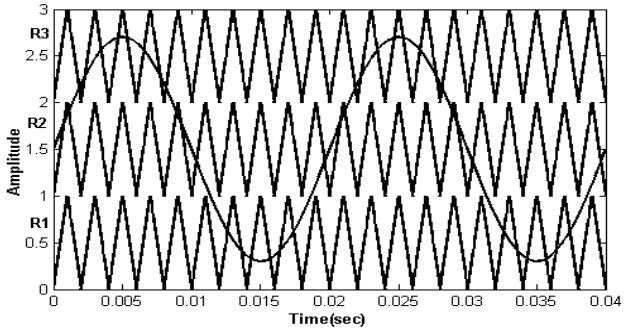

Fig. 2 Different regions in carrier comparison approach

Let us consider Vc be the amplitude of triangle wave and V_m be the amplitude of reference wave. Now we define modulation index as

$$M_i = \frac{Vm}{V_C(N-1)} \tag{3}$$

If the modulation signal lies within the region R_1 as shown in Fig. 3, only Inverter-I is in operation and inverter-II is clamped.

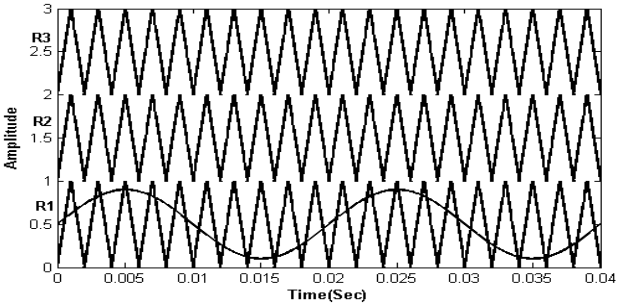

Fig. 3 Modulation signal position during two-level operation

All the phases of inverter-I produces a two-level output voltage ($V_{dc}/3$ or $2V_{dc}/3$) by operating switches (S_1, S_3, S_5) and (S_2, S_4, S_6) and clamping the switches (S_7, S_9, S_{11}) to a voltage of positive voltage of $V_{dc}/3$. The corresponding pole voltages, phase voltages and line voltages are shown in Fig. 4.

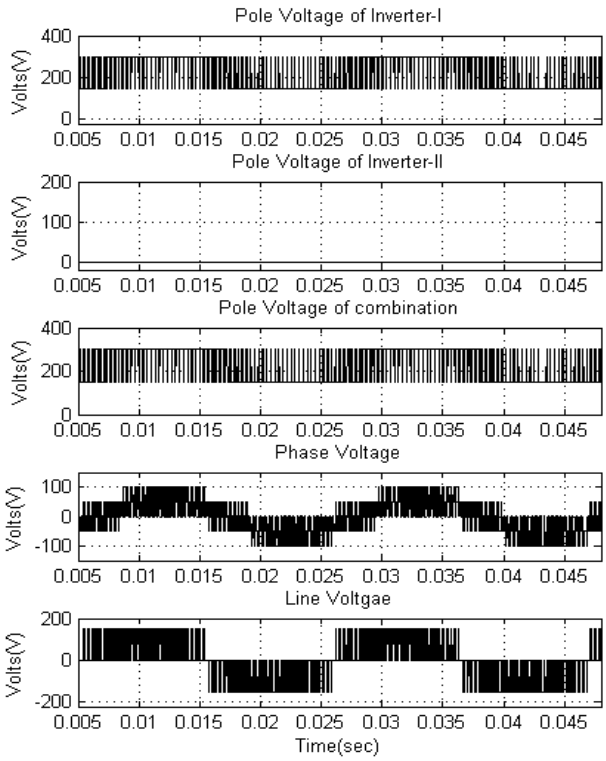

Fig. 4 Voltage plots during two-level operation by using the SPWM algorithm

As the combined pole voltage of the proposed inverter produces two-level output the mode of operation is called as two-level operation. If the modulating wave is present in both regions R_1 and R_2 as shown in Fig. 5, all the switches in inverter-I operate continuously to produce output voltage. When switches (S_1, S_3, S_5) and (S_7, S_9, S_{11}) are ON Inverter-I produces an output voltage of ($2V_{dc}/3$). When (S_2, S_4, S_6) and (S_7, S_9, S_{11}) are ON inverter-I produces an output voltage of ($V_{dc}/3$). When (S_8, S_{10}, S_{12}) are ON, inverter-I produces zero output voltage. Similarly, all the switches in inverter-II are clamped to produce a zero voltage.

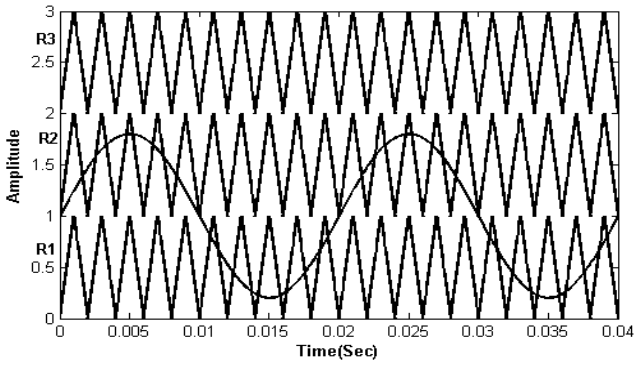

Fig. 5 Modulating signal during three-level operation

Therefore the effective pole voltage of proposed multilevel inverter contains three levels ($2V_{dc}/3$, $V_{dc}/3$, 0). So this mode of operation is known as three-level mode of operation. The corresponding pole voltages, phase voltages and line voltages are shown in Fig. 6 during three-level mode of operation.

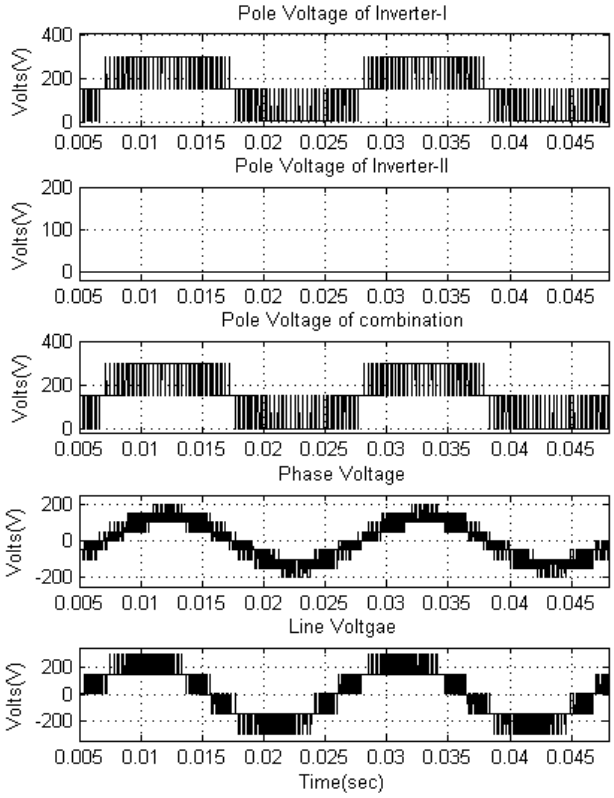

Fig. 6 Voltage plots during three-level operation by using the SPWM algorithm

When the modulating signal is present in all the three regions as shown in Fig.2 all the switches in proposed multilevel inverter topology operate continuously to produce an output voltage. During this mode of operation inverter-I produce three-level output voltage and inverter-II produce two-level output voltage. The corresponding pole voltages of inverter-I and inverter-II during this mode of operation are given in Table-1 along with their effective pole voltages. Thus a three phase induction motor attains four-level output voltages. So the combined effective pole voltage of proposed multilevel inverter produces four-level output voltage as shown in Fig. 7. The corresponding pole voltages, phase voltages and line voltages during four level operations are shown in Fig. 7.

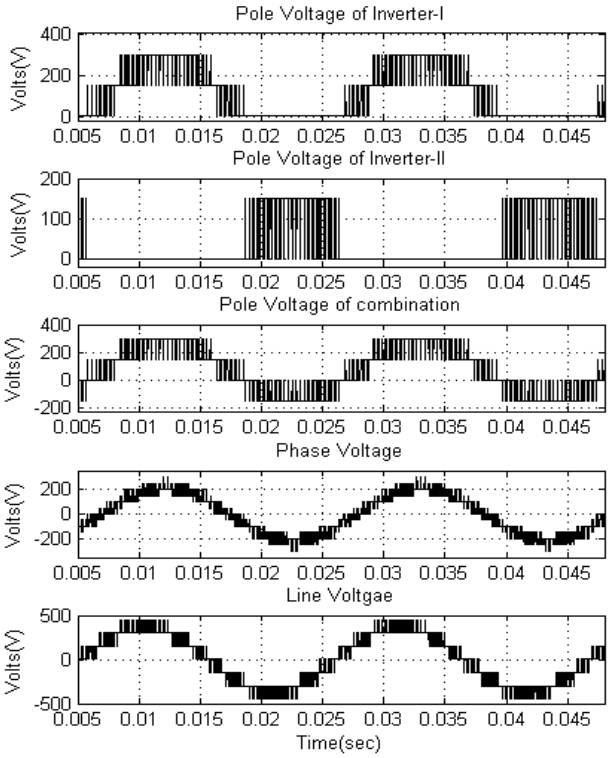

Fig. 7 Voltage plots during four-level operation by using the SPWM algorithm

Table 1 Different voltages during four-level operation

Pole voltage of inverter-I V_{a10}	Pole voltage of Inverter-II V_{a20}	Effective pole voltage V_a
0	0	0
0	$V_{dc}/3$	$-V_{dc}/3$
$V_{dc}/3$	0	$+V_{dc}/3$
$V_{dc}/3$	$V_{dc}/3$	0
$2V_{dc}/3$	0	$+2V_{dc}/3$
$2V_{dc}/3$	$V_{dc}/3$	$+V_{dc}/3$

The advantage of proposed control strategy for proposed multilevel inverter topology is that all the four levels of operation can be achieved in entire modulation index (from 0 to1).

3. PROPOSED GPWM ALGORITHM

Assume two set of instantaneous phase voltages as given in (4) and (5).

$$\begin{aligned} V_{an} &= V_m \cos(\omega t) \\ V_{bn} &= V_m \cos(\omega t - 120) \\ V_{cn} &= V_m \cos(\omega t - 240) \end{aligned} \tag{4}$$

$$\begin{aligned} V_{ax} &= V_m \cos(\omega t) \\ V_{bx} &= V_m \cos(\omega t - 120) \\ V_{cx} &= V_m \cos(\omega t - 240) \end{aligned} \tag{5}$$

As the potential O and O' are isolated, in proposed GPWM algorithm, the modulating waves are generated by simply adding zero sequence voltage to the instantaneous phase voltages as given in (6).

$$V_{in}^{*} = V_{in} + V_{zs}, \quad i = a,b,c \tag{6}$$

$$\text{Where } V_{zs} = \frac{Vdc}{2}(2a_0 - 1) - a_0 V_{\max} + (a_0 - 1) \tag{7}$$

V_{zs} is known as zero sequence voltage.

V_{max} is the maximum of V_{an}, V_{bn}, V_{cn} and $V_{max,x}$ is the maximum value of V_{ax}, V_{bx}, V_{cx} in each sampling time interval. For the generation of various PWM algorithms, the variation of the constant is shown in Table-2 and the corresponding modulating signals are shown in Fig. 8. From the Fig. 8, it can be observed that the SVPWM has continuous modulating waveform and hence gives continuous pulse pattern. Whereas, the modulating waves of discontinuous PWM (DPWM) algorithms clamp to either positive dc or negative dc bus for a duration of 120 degrees in each fundamental cycle. Hence, the switching losses can be reduced by 33.33%.

Table 2 a_o value for various PWM algorithms

PWM algorithm	a_o
SVPWM	0.5
DPWMMIN	0
DPWMMAX	1
DPWM0	$V_{\max} + V_{\min} < 0$ then $a_0 = 0$ $V_{\max} + V_{\min} \geq 0$ then $a_0 = 1$
DPWM1	$V_{\max,x} + V_{\min,x} \geq 0$ then $a_0 = 1$ $V_{\max,x} + V_{\min,x} < 0$ then $a_0 = 0$
DPWM2	$V_{\max} + V_{\min} < 0$ then $a_0 = 1$ $V_{\max} + V_{\min} \geq 0$ then $a_0 = 0$
DPWM3	$V_{\max,x} + V_{\min,x} < 0$ then $a_0 = 1$ $V_{\max,x} + V_{\min,x} \geq 0$ then $a_0 = 0$

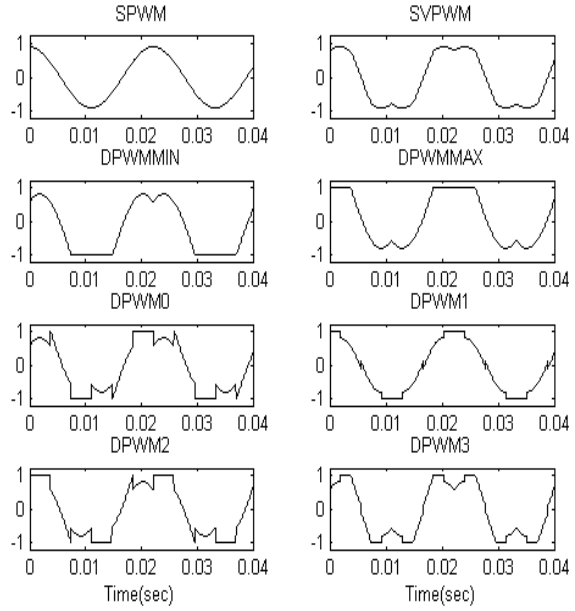

Fig. 8 Modulating signals of different PWM algorithms

4. SIMULATION RESULTS AND DISCUSSION

The characteristics of multilevel inverter topology with different PWM algorithms have been studied and analyzed in MATLAB/simulation environment for a three phase induction motor. The induction motor parameters used in the analysis and inverter parameters are given in Table-3. For the simulation studies, the switching frequency is taken as 3 kHz. Hence, the sampling time period (T) for is taken as 0.333ms. The simulation studies have been carried out for four-level operation. Hence, to achieve four -level operation, for a sampling time period of T inverter-I is switched for a period of (2T/3) and inverter-II is switched for a period of (T/3). Moreover, when one inverter is switched other inverter is clamped. The operation of inverters for various PWM algorithms is as shown in Table-4. The simulation results for various PWM algorithms for a four-level operation are shown in from Fig. 9 to Fig. 15.

Table 3 Parameters and specifications of the Induction motor

Rated speed	1500 RPM	Rotor resistance	1.21Ω
frequency	50HZ	Inverter input DC Voltage	450V
Stator resistance	1.57Ω	Mutual inductance	176mH
Stator inductance	183mH	Rotor inductance	183mH

Table 4 Operation of inverters for various PWM algorithms

Type of PWM	Operation of Inverter-I in 2T/3 time period	Operation of Inverter-II in T/3 time period	Reason
SPWM	Continuous switching in2T/3 period	Continuous switching in T/3 period	Continuous modulating waveform
SVPWM	Continuous switching in2T/3 period	Continuous switching in T/3 period	Continuous modulating waveform
DPWMMIN	clamped for some time duration in 2T/3 period	Continuous switching in T/3 period	As the modulating wave is clamped to negative dc bus
DPWMMAX	Continuous switching in 2T/3 period	clamped for some time duration in T/3 period	As the modulating wave is clamped to positive dc bus
DPWM0	clamped for some time duration in 2T/3 period	clamped for some time duration in T/3 period	As the modulating wave is clamped to both positive and negative dc bus
DPWM1			
DPWM2			
DPWM3			

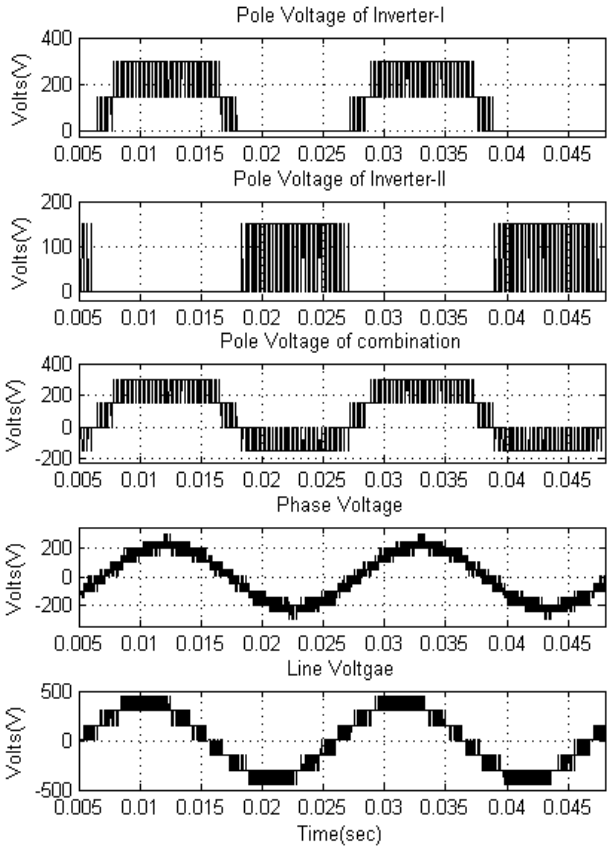

Fig. 9 Voltage plots with SVPWM algorithm during four-level operation

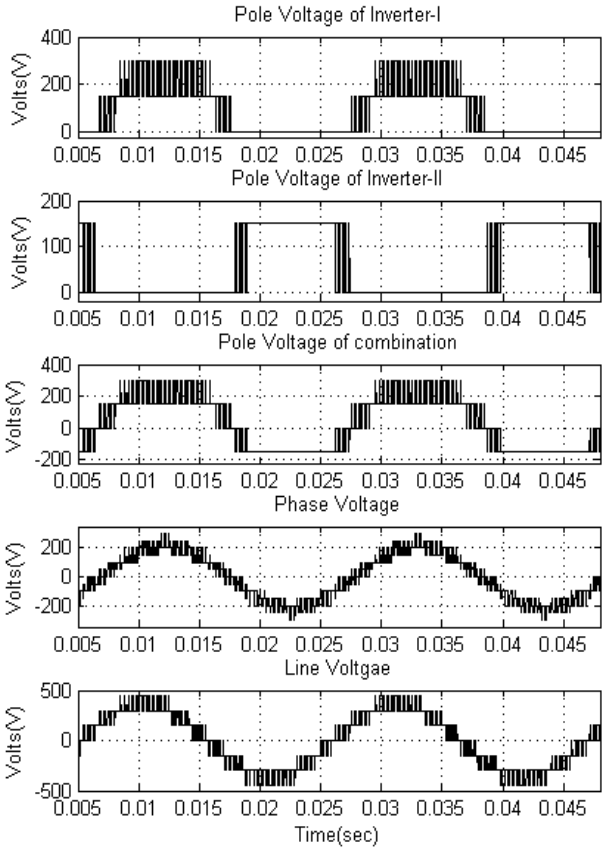

Fig. 11 Voltage plots with DPWMMAX algorithm during four-level operation

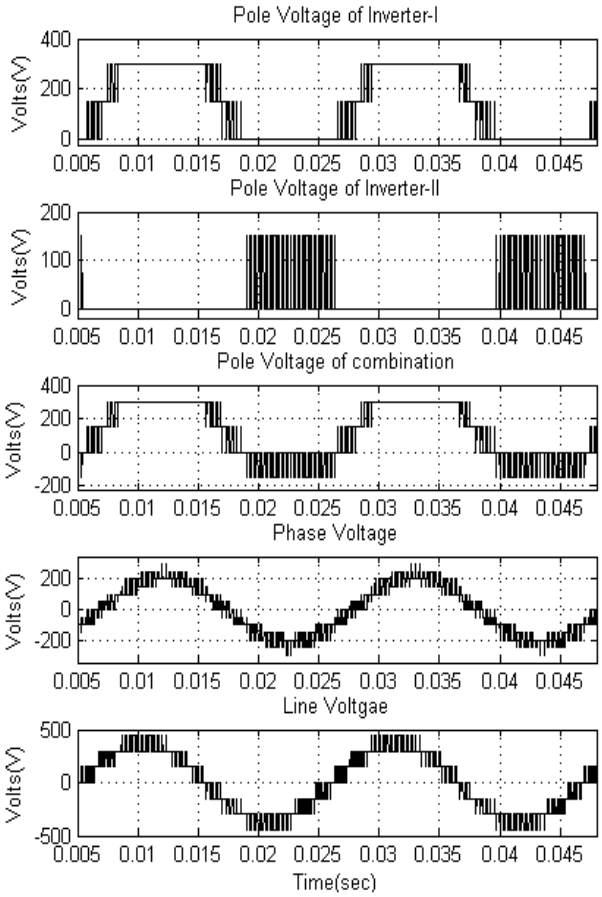

Fig.10 Voltage plots with DPWMMIN algorithm during four-level operation

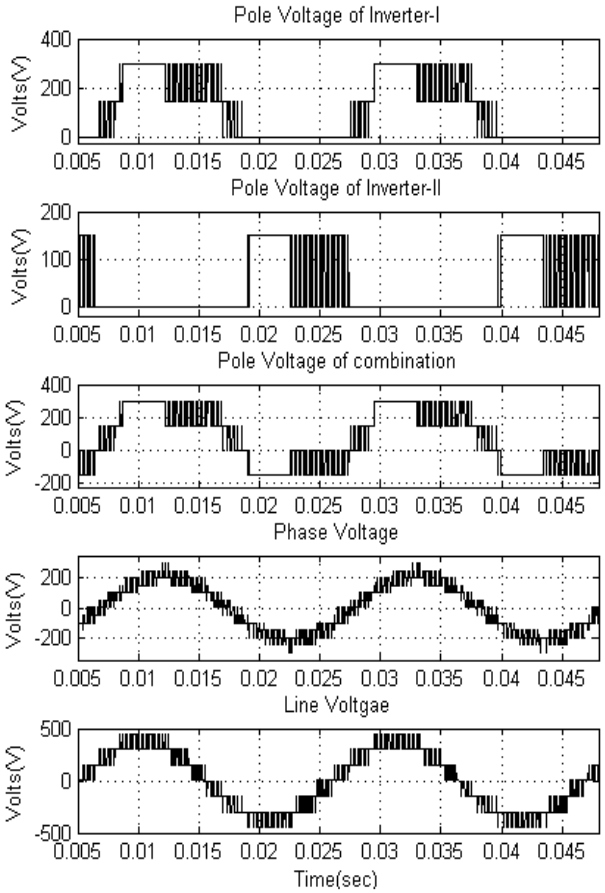

Fig. 12 Voltage plots with DPWM0 algorithm during four-level operation

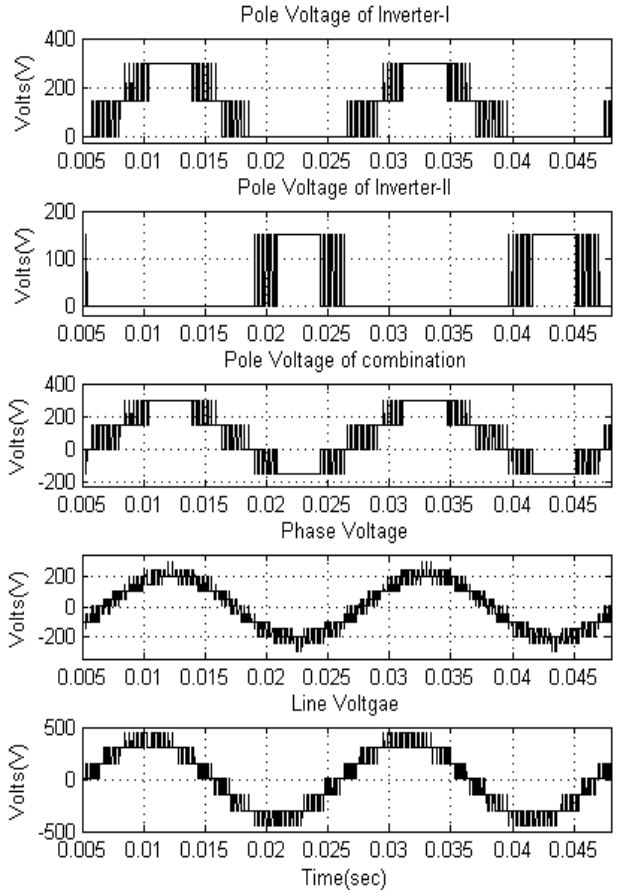

Fig. 13 Voltage plots with DPWM1 algorithm during four-level operation

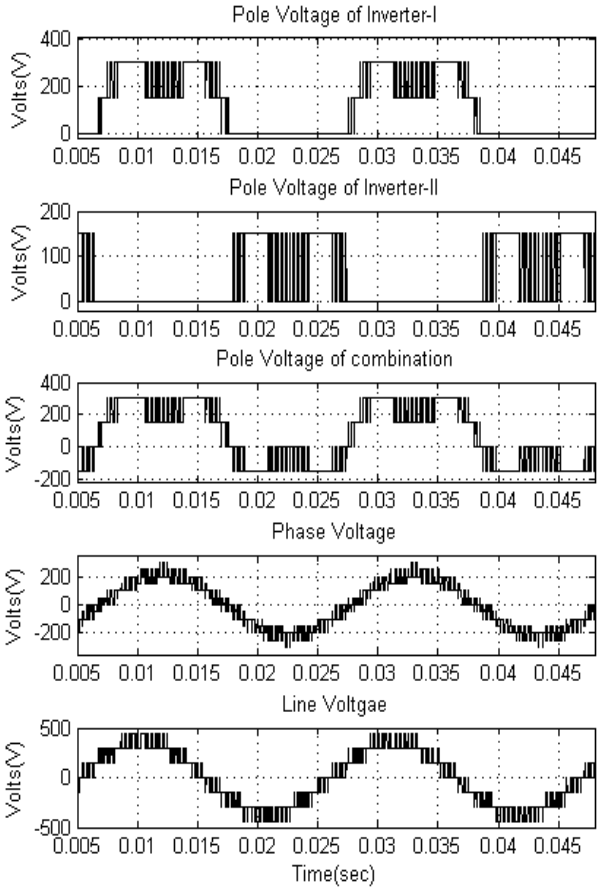

Fig. 15 Voltage plots with DPWM3 algorithm during four-level operation

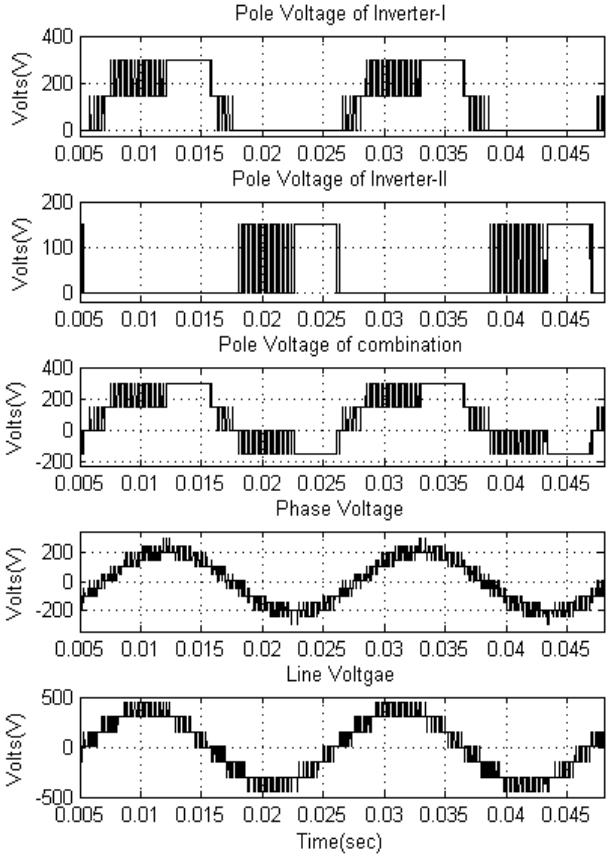

Fig. 14 Voltage plots with DPWM2 algorithm during four-level operation

The harmonic spectra of line voltages for various PWM algorithms are shown in from Fig. 16 to Fig. 23 for four-level operation. Moreover, the harmonic spectra line voltage for two-level and three-level operation with SPWM algorithm is shown in Fig. 24 and Fig. 25. From the harmonic spectra results, it can be observed that as the number of levels increases, the harmonic distortion also decreases. Moreover, the proposed GPWM algorithm gives all possible PWM algorithms with reduced complexity. Also, it can be concluded that as the DPWM algorithms clamp for a total period of 120 degrees in each fundamental cycle, the switching losses can be reduced 33.33%.

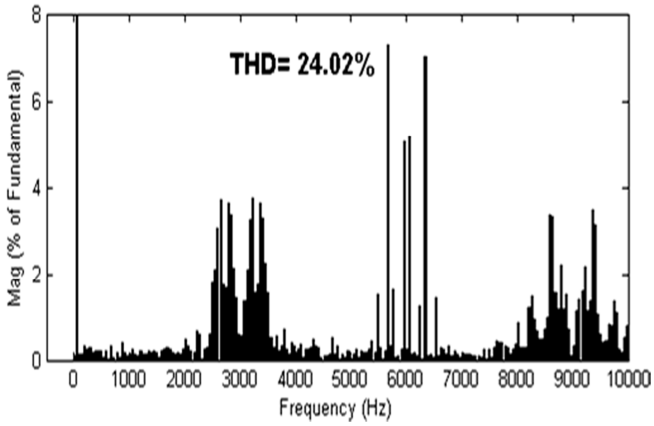

Fig. 16 Harmonic spectra of line voltage for SPWM algorithm

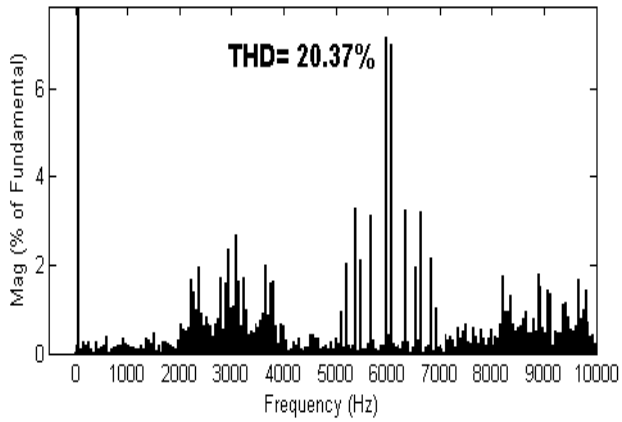

Fig. 17 Harmonic spectra of line voltage for SVPWM algorithm

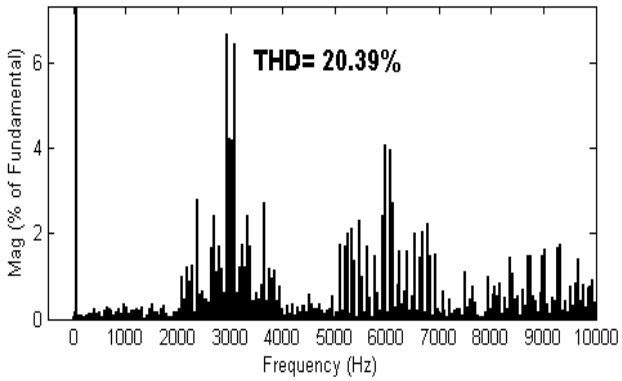

Fig. 18 Harmonic spectra of line voltage for DPWMMIN algorithm

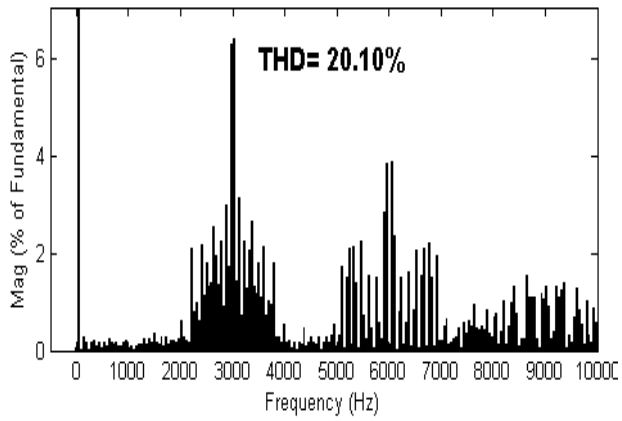

Fig. 19 Harmonic spectra of line voltage for DPWMMAX algorithm

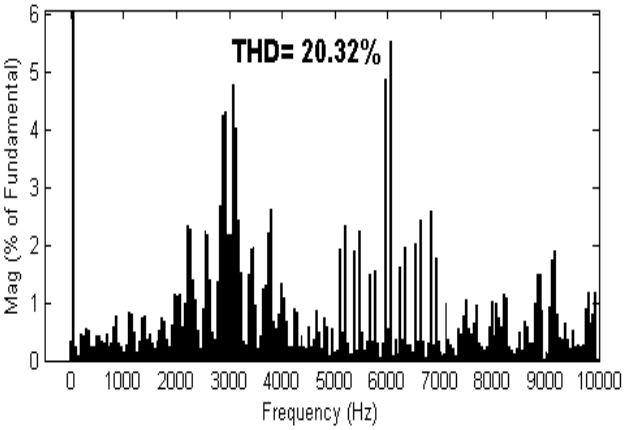

Fig. 20 Harmonic spectra of line voltage for DPWM0 algorithm

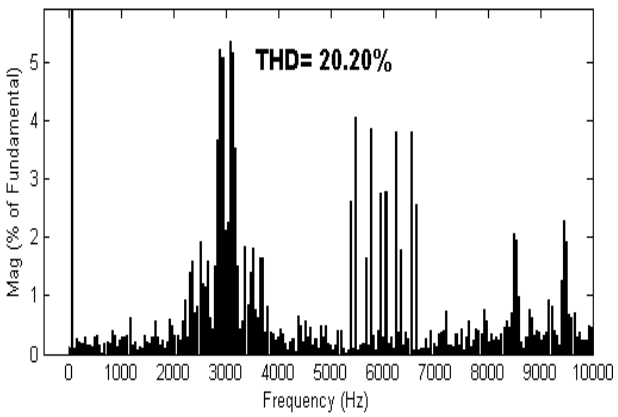

Fig. 21 Harmonic spectra of line voltage for DPWM1 algorithm

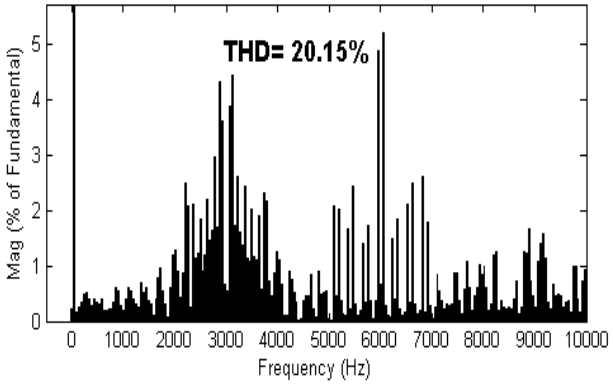

Fig. 22 Harmonic spectra of line voltage for DPWM2 algorithm

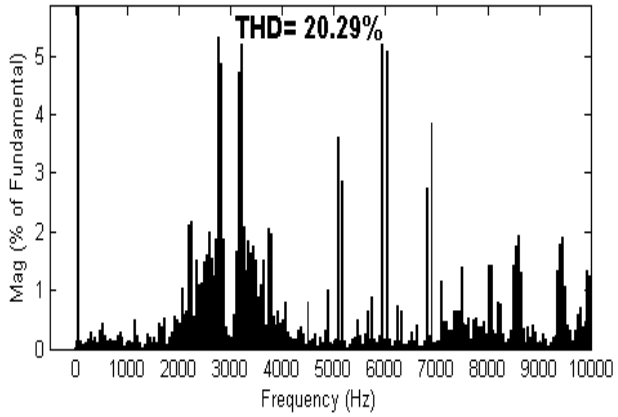

Fig. 23 Harmonic spectra of line voltage for DPWM3 algorithm

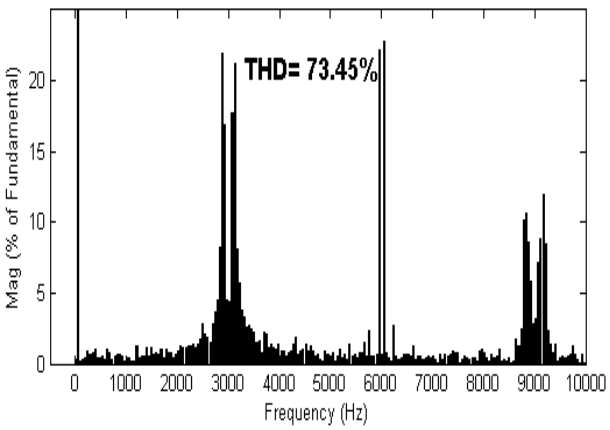

Fig. 24 Harmonic spectra of line voltage for SPWM algorithm for two-level operation.

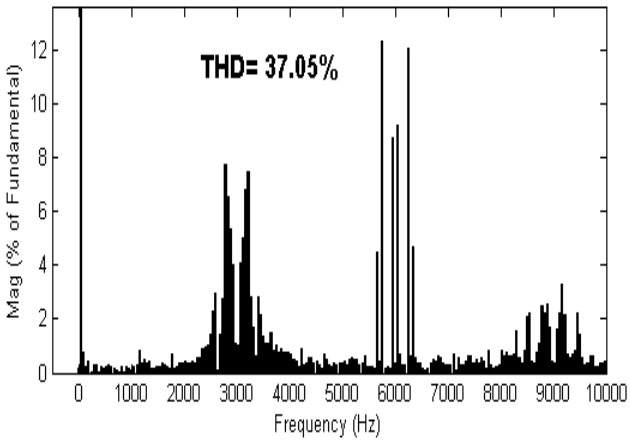

Fig. 25 Harmonic spectra of line voltage for SPWM algorithm for three-level operation.

5. CONCLUSIONS

The proposed GPWM algorithm is very simple and is less complex when compared to conventional continuous and discontinuous PWM algorithms. From the results it can be concluded that discontinuous PWM techniques reduce a total of 33% of switching losses when compared to continuous PWM algorithms. Moreover, the proposed circuit topology can generate two-level, three-level and four-level output voltages with reduced switching losses at all the modulation indices. As number of levels increases harmonic content in the output voltage gets reduced. In view of performance the proposed inverter topology is highly efficient at low voltage rating also. During faulty conditions of the drive the complete motor drive can be operated with one set of inverter by isolating other inverter from the operation.

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