SPACE VECTOR BASED RANDOM DISCONTINUOUS PWM SCHEMES FOR VSI FED AC DRIVE FOR REDUCED HARMONIC DISTORTION, ACCOUSTIC NOISE AND SWITCHING LOSS

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ABSTRACT

This paper presents space vector based random discontinuous PWM techniques for two level three phase inverter fed induction motor drive. The pulse width modulation (PWM) based induction motor drives often produces objectionable acoustic noise apart from harmonic distortion. The proposed modulation techniques not only concentrate on harmonic reduction through reduced switching but also aim at acoustic noise reduction which causes inconvenience in certain applications such as electric propulsion for the drivers and passengers. The proposed algorithm is developed by using the imaginary switching times, which does not require angle and sector information. In order to get the randomization effect, the proposed algorithm uses discontinuous pulse width modulation algorithm in conjunction with the variable delay pulse width modulation (VDRPWM) algorithm. The proposed PWM algorithm uses 012 and 721 sequences results 33.33% reduction in inverter switching loss, as the zero state time is varied randomly according to the operating sequence, randomization effect will occur, which results in reduced total harmonics distortion and hence gives reduced acoustical noise. To validate the proposed PWM algorithm, the numerical simulation studies have been carried out and results are presented and compared. The simulation results confirm the effectiveness of the proposed algorithm.

Keywords: *acoustic noise, SVPWM, harmonic distortion, Variable Delay Random PWM (VDRPWM), DPWM*

1. INTRODUCTION

It is proven well that the voltage source inverter fed drives are more popular in industrial applications. With the advancement in control strategies of induction motor drives, PWM algorithms finds an immense growth in motor drive applications and it is possible to reduce switching losses and total harmonic distortion content. Many PWM control strategies have been described in [1-3], out of which well-known methods are Sinusoidal PWM (SPWM) and Space Vector PWM (SVPWM).Any ac drive needs full utilization of dc bus voltage for achieving high torque under all operating conditions. In this aspect SPWM method for VSI works satisfactorily to some extent. However Space vector based PWM (conventional) results in better dc bus utilization [4]. Apart from this the current ripple in steady state operation and also harmonic distortion will be reduced when conventional SVPWM is employed. A brief review of conventional SVPWM is as follows.

Fig. 1 shows the voltage vectors produced by a three-phase, two-level inverter, with six active voltage vectors dividing the space vector plane into six sectors. In CSVPWM algorithm, the desired reference voltage vector is generated by time averaging the suitable discrete voltage vectors in every sub cycle or sampling time period T_s. For example, the reference vector in sector I, as shown in Fig. 1, is generated by applying the active state 1, active state 2 and the zero states 0 and 7 for durations T1, T2 and TZ respectively [5].

For a given reference voltage vector and Ts, the duration T1, T2 and TZ are unique. The expressions for the various active state time durations and zero states time duration in the first sector can be given as in formulae (1)-(3).

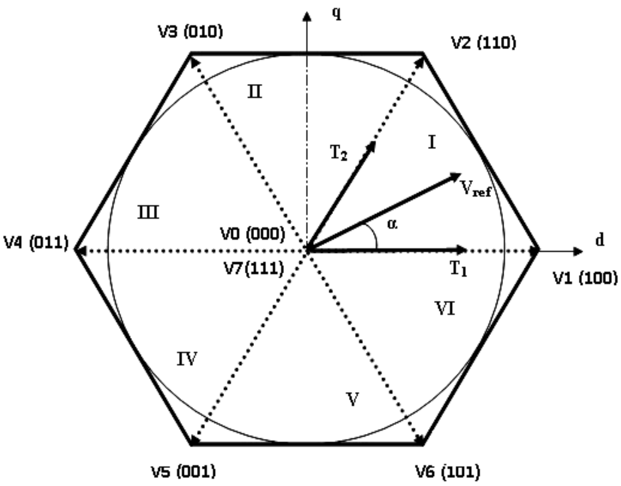

Fig. 1 Voltage space vectors for SVPWM

$$T_1 = \frac{2\sqrt{3}}{\pi} M_i \left(\sin(60^o - \alpha)\right) T_s \tag{1}$$

$$T_2 = \frac{2\sqrt{3}}{\pi} M_i \left(\sin \alpha\right) T_s \tag{2}$$

$$T_Z = T_s - T_1 - T_2 \tag{3}$$

where $M_i = \frac{\pi V_{ref}}{2V_{dc}}$

The active states for the inverter can be represented as follows.

$$V_k = \frac{2}{3} V_{dc} e^{j(k-1)\frac{\pi}{3}} \quad \text{where } k = 1, 2, \ldots, 6$$

Different switching sequences can be obtained by using conventional space vector approach as given in (1)-(3), which uses the reference voltage vector and angle information. This basic CSVPWM is the base for further developments of SVPWM algorithms. Many researchers are striving hard and continuing their efforts to improve drive performance with the advancement in technological developments [6]. Though SVPWM algorithms give good performance, it is not able to reduce some of the problems as mentioned below.

One of the problems in PWM based VSI fed drives is the acoustic noise which is due to small amount of vibration caused by normal electromagnetic and mechanical forces inside the motor and it is very much objectionable in silent environments. The harmonic spectrum of PWM source is high and associated switching frequency has direct effects on motor acoustics [7]. In some applications, a motor may produce an objectionable level or frequency of noise when operating on PWM drive power. It is not possible to accurately predict the total noise level for any given motor but can be limited to an acceptable level by applying either reduced V/Hz operation in variable torque applications or operating at the optimum switching frequency. Also critical frequency avoidance adjustment can be used, which is of less significance. Among the methods listed above, optimum switching frequency is suggest able that is done by raising or lowering the switching frequency which results in harmonic current reduction and in turn resulting in reduction of the sound level perceived. Increasing the switching frequency usually reduces the noise produced by the motor. But it has a disadvantage of power loss in switching devices. Hence to overcome switching loss, discontinuous PWM sequences are being employed instead of continuous PWM methods with fixed switching frequencies. To make use of optimum switching and to reduce switching loss along with acoustic noise, random switching frequency may be employed as explained in [8] in Discontinuous PWM sequences. In the subsequent sections of this paper, operating principle of variable delay random technique for randomization of switching periods along with Discontinuous PWM methods are described.

2. VARIABLE DELAY RANDOM TECHNIQUE

The ideal random PWM (RPWM) algorithm should possess reduced acoustic noise over the full operating range, easier implementation, reduced complexity, acceptable switching losses and minimal impact on the system dynamics and basic motor control functionality. The RPWM algorithms can be classified into two categories as random switching frequency PWM (RSFPWM) and fixed switching frequency PWM algorithms. In the RSFPWM algorithms, both the sampling and PWM periods are synchronized. The major drawback of the RSFPWM algorithm is the limitation of the maximum code size by the minimum sampling time period. The fixed switching frequency RPWM algorithms can be classified as random zero state distribution PWM (RZSDPWM), random center distribution PWM (RCDPWM) and random lead-lag PWM (RLLPWM) algorithms. Though the fixed switching frequency RPWM algorithms allow optimal use of the processor computational capability due to fixed sample rate, these suffer from few limitations. RZSDPWM and RCDPWM algorithms lose effectiveness at higher modulation indices. The RLLPWM algorithm does not offer a very good performance with respect to the reduction of acoustic/EMI emissions and suffers an increased current ripple as well. Additionally, both RLLPWM and RCDPWM introduce an error in the fundamental component of current due to a per-cycle average value of the switching ripple. Hence, VDRPWM algorithms are used in this paper for direct torque controlled induction motor drive. However, the existing VDRPWM algorithm uses sector and angle information for the calculation of gating times, which increase the complexity. Hence, to reduce the complexity involved in the algorithm, the concept of imaginary switching times is used and the gating times are calculated as explained in the previous section.

If either the pulse position or the switching frequency is varied in a random manner, the power spectrum of the output voltage of the converter acquires a continuous part, while the discrete (harmonic) part is significantly reduced. This is the basic principle of the random pulse width modulation (RPWM) which has in recent years attracted the increasing interest of researchers. The detailed review of the RPWM algorithms is given in [9]. Among, various RPWM algorithms, random pulse position PWM algorithms are easier for implementation [7-10]. However, a novel algorithm known as variable delay RPWM (VDRPWM) is reported recently. The VDRPWM algorithm is characterized by a constant switching frequency and a varying switching period (Ts) realized by random changes of the delay of switching cycles with respect to the corresponding sampling cycles. However, the existing VDRPWM algorithm requires angle and sector information, which increases the complexity involved in the algorithm. To reduce the complexity involved in the conventional space vector approach, various PWM algorithms have been developed in [10] by using the concept of imaginary switching times.

This paper presents a space vector based variable delay PWM algorithms, namely variable delay random SVPWM (VDRSVPWM), variable delay random DPWMMIN (VDRDPWMMIN) and variable delay random DPWMMAX (VDRDPWMMAX) algorithms. All the proposed VDRPWM algorithms use fixed sample rate for optimal usage of processor computational power while providing quasi-random PWM output for good spectral spreading. This algorithm introduces a random delay into the trailing edge of the next PWM output cycle. Since two consecutive edges determine the PWM output period, a quasi-random PWM output is created as shown in Fig. 2. The detailed flowchart of the proposed VDRPWM algorithms is shown in Fig. 3, which illustrates the computation of the delay and switching period within the processor. In the proposed VDRPWM algorithms, a random number is generated between 0 and 1. Then, this is multiplied by sample time period to obtain the random delay time. Hence, the delay time is varied from zero to sampling time period. To avoid very short output PWM periods, a lower limit on the switching period is defined as minimum sampling time period (Tswmin). If the initial switching period calculation is less than the Tswmin, it will be clamped to *T*swmin. Hence, the final delay must be recalculated after the limiting function. Thus, the resultant switching period may vary from *T*swmin to 2 times the sampling time period. The average switching period will equal the sample period over time.

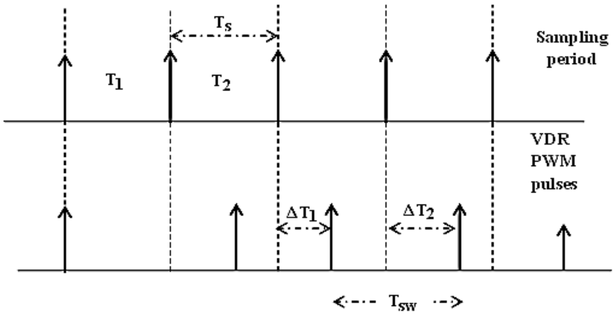

Fig. 2 Timing diagram for VD-RPWM implementation

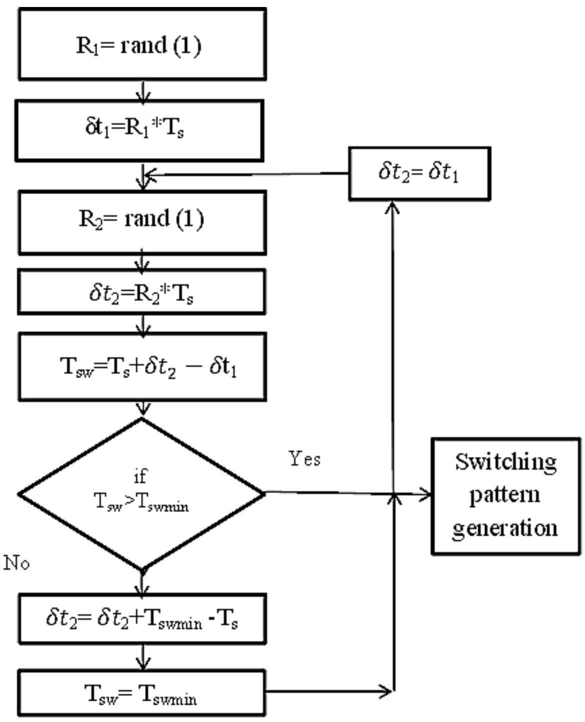

Fig. 3 Flow chart of a VDPWM algorithm

The VDRPWM algorithms do not affect the basic motor control algorithm or type of space vector modulation employed. Thus, the VDRPWM algorithms consist of two steps. First, the duty cycles of various PWM algorithms are computed as given in previous section with fixed frequency. In second step, the delay is now computed as well. Then the duty cycles and delay are passed to the PWM modulator.

Thus, the VDRPWM algorithms can be added to the inverter with minimal impact on the motor control algorithm. The switching loss of the inverter is also same as existing deterministic PWM algorithms.

Moreover, as it uses fixed sample rate, it avoids the updating of filter and regulator gains, which is necessary when using variable sample rate techniques.

3. PROPOSED VARIABLE DELAY RANDOM DISCONTINUOUS PWM SCHEME

SVPWM algorithm distributes the zero state time equally in every sampling time period. By utilizing the unequal distribution of zero voltage vector switching times, various PWM algorithms can be generated. To generate the proposed switching sequences, the zero state time durations can be modified as $T0 = \mu\ Tz$ for V0 voltage vector and $T7 = (1- \mu)Tz$ for V7 voltage vector. By varying the μ value between 0 and 1, various discontinuous PWM algorithms can be generated. The SVPWM, DPWMMIN and DPWMMAX algorithms can be generated for μ =0.5, 1 and 0 respectively. These algorithms use 0127-7210, 012-210 and721-127 sequences in the first sector and so on. In each sampling time interval, the SVPWM algorithm has three number of switchings and whereas for the DPWMMAX algorithm is two. Hence, to get the same average switching frequency of the inverter, a sampling time interval is taken as $Ts = T$ for the SVPWM algorithm, while $Ts = (2T/\ 3)$ for the Discontinuous algorithm [11-15].

The use of DPWM schemes reduces 33% of the switching loss of the inverter, it means that number of on and off of the inverter switch is reduced by 33% by clamping each of the pole voltage to either positive bus or negative bus for a period of 120°.

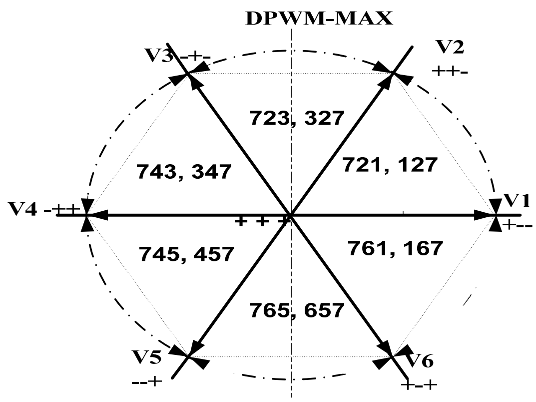

Fig. 4 Voltage space vectors for DPWMMAX

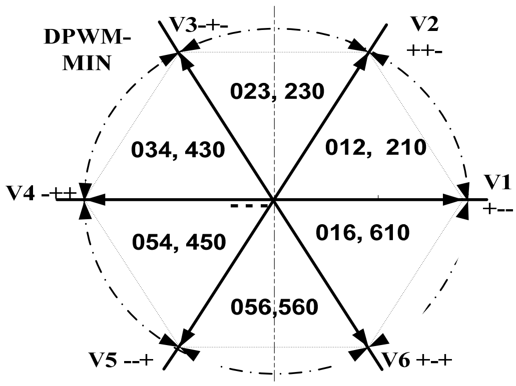

Fig. 5 Voltage space vectors for DPWMIN

The proposed discontinuous algorithm is implemented in conjunction with variable delay random PWM algorithm for three phase two level inverter [16-18].

Table 1 shows the generation of various Pulse Width Modulation (PWM) Modulating signals with the variation of zero sequence component (μ) value.

Table 1 Switching sequences for CSVPWM, DPWMIN and DPWM MAX in all sectors

Sector	CSVPWM	DPWMMIN	DPWMMAX
I	0127-7210	012-210	721-127
II	0327-7230	032-230	723-327
III	0347-7430	034-430	743-347
IV	0547-7450	054-450	745-547
V	0567-7650	056-650	765-567
VI	0167-7610	016-610	761-617

4. SIMULATION RESULTS AND DISCUSSION

To verify the proposed random discontinuous PWM methods, numerical simulation studies have been carried out using Matlab. For the simulation, the average switching frequency of the inverter is taken as 3 kHz. The induction motor used in this case study is a 1.5 kW, 1440 rpm, 4-pole, 3-phase induction motor having the following parameters:
Rs = 7.83 Ω, Rr = 7.55 Ω, Ls = 0.4751 H, Lr = 0.4751 H, Lm = 0.4535 H and J = 0.06 Kg.m2

The steady state simulation results of conventional SVPWM algorithm, DPWMIN and DPWMAX without random PWM scheme are shown in Fig. 6 and Fig. 14. From which, it can be observed that the amplitudes of dominating harmonics around switching frequency are high in SVPWM algorithm; it gives more acoustical noise and harmonic distortion. To reduce acoustical noise, the discontinuous VDRPWM algorithms are proposed in this paper. The steady state simulation results of proposed VDRSVPWM, VDRDPWMMIN and VDRDPWMMAX algorithms are shown in from Fig. 15 to Fig. 23.

From the simulation results, it can be observed that the proposed VDRPWM algorithms give reduced THD when compared with the SVPWM algorithms. Moreover, as the amplitude of dominating harmonics is less when compared with the classical SVPWM algorithms, the proposed VDRPWM algorithms give less acoustical noise. Moreover, the proposed VDRPWM algorithms give spread spectra when compared with the SVPWM algorithm.

Though the Space Vector based PWM algorithms for VSI fed induction motor drive gives good performance, it generates more acoustical noise and harmonic distortion due to the dominating harmonics around the multiples of switching frequency. Hence, to reduce the harmonic distortion and acoustical noise of the drive, VDRPWM algorithms are proposed for voltage source inverter fed induction motor drive. From Fig. 24 it observed that magnitude of acoustic noise (in db) is around -80db for without random PWM where as it is around -70 db for Random PWM Algorithm.

A. Steady state plots of SVPWM (Without Random)

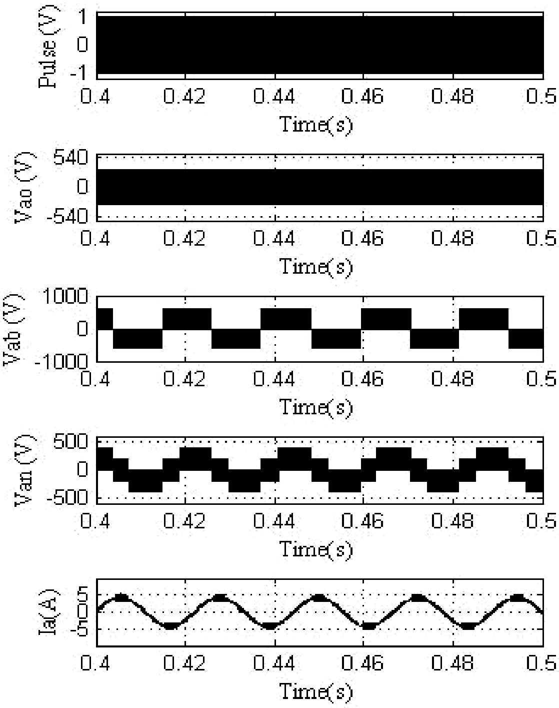

Fig. 6 Pulses, Pole voltage, Line voltage, Phase voltage and stator current

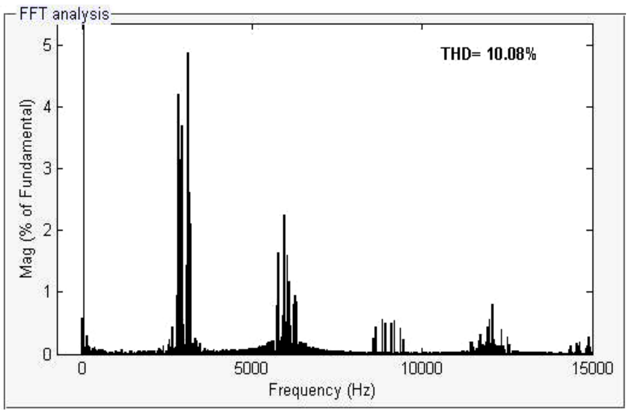

Fig. 7 THD analysis of stator current

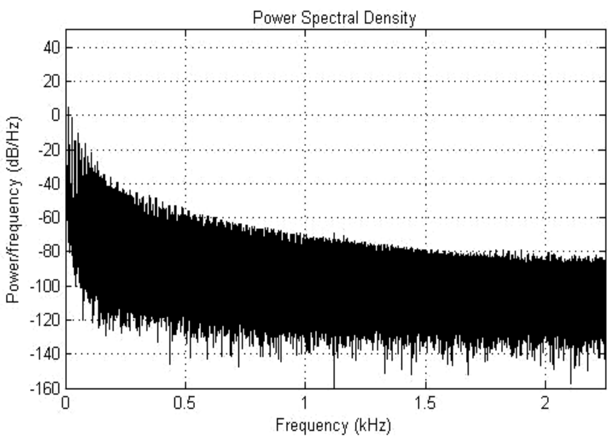

Fig. 8 Acoustic noise for SVPWM

B. Steady state plots of DPWMMIN (Without Random)

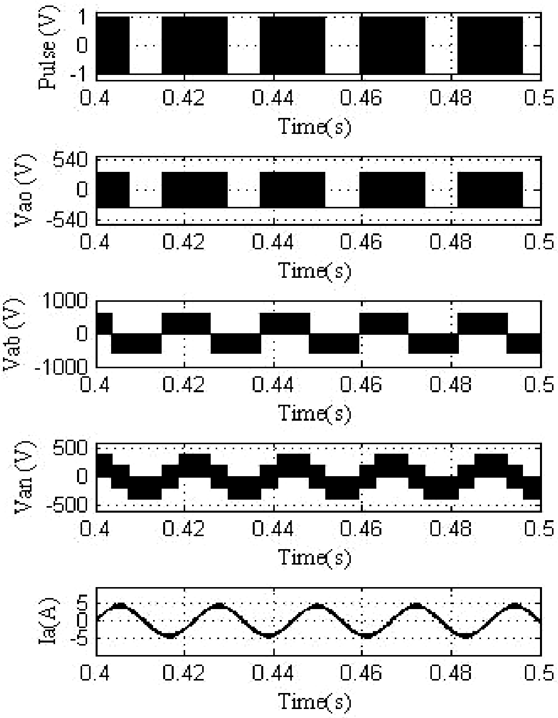

Fig. 9 Pulses, Pole voltage, Line voltage, Phase voltage and stator current

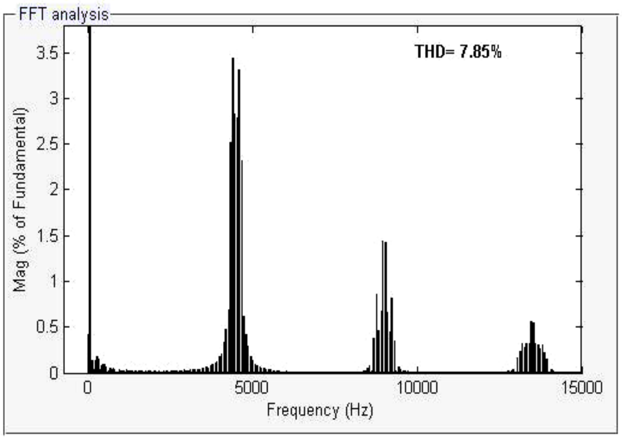

Fig. 10 THD analysis of stator current

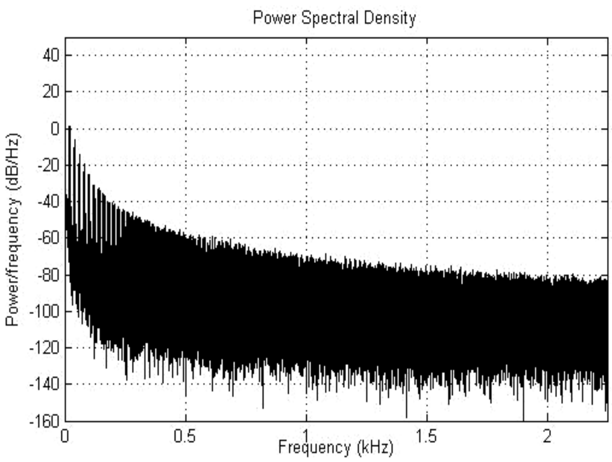

Fig. 11 Acoustic noise for DPWMMIN

C. Steady state plots of DPWMMAX (Without Random)

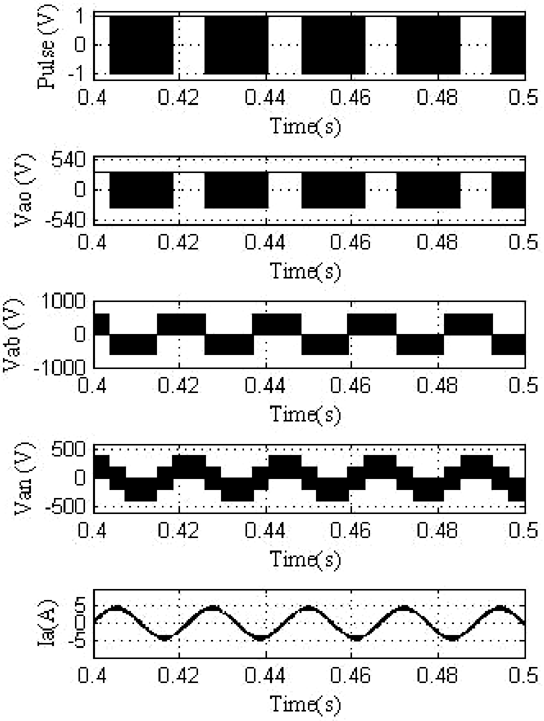

Fig. 12 Pulses, Pole voltage, Line voltage, Phase voltage and stator current

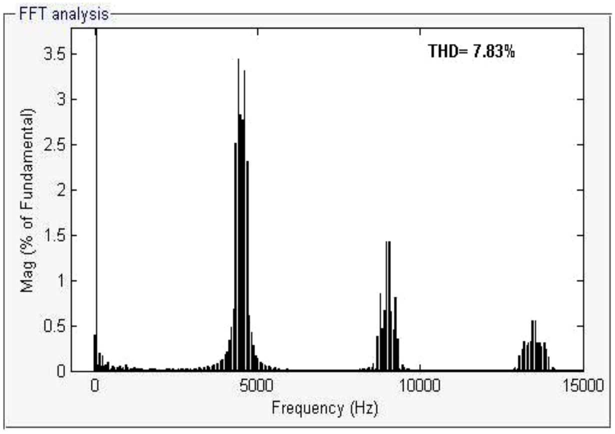

Fig. 13 THD analysis of stator current

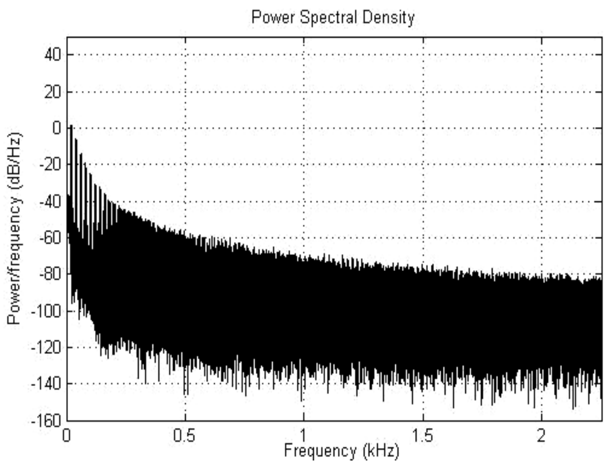

Fig. 14 Acoustic noise for DPWMMAX

D. Steady state plots of VDR SVPWM (With Random)

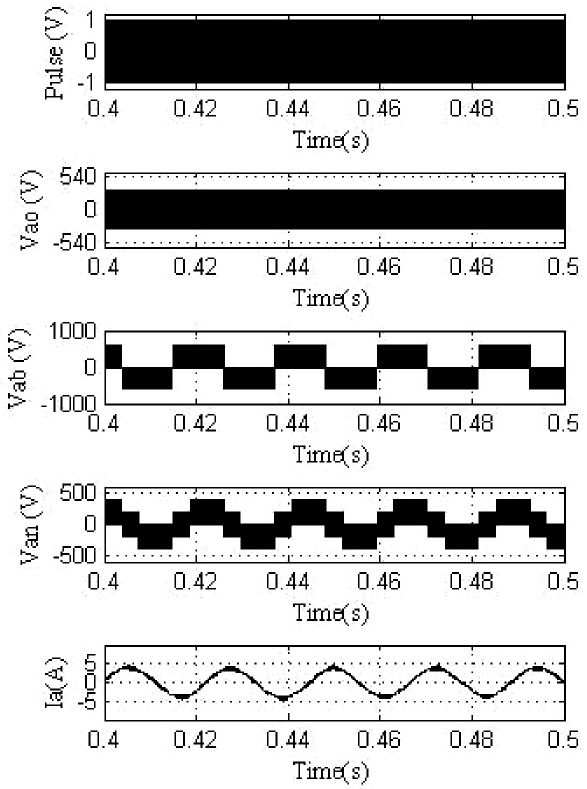

Fig. 15 Pulses, Pole voltage, Line voltage, Phase voltage and stator current

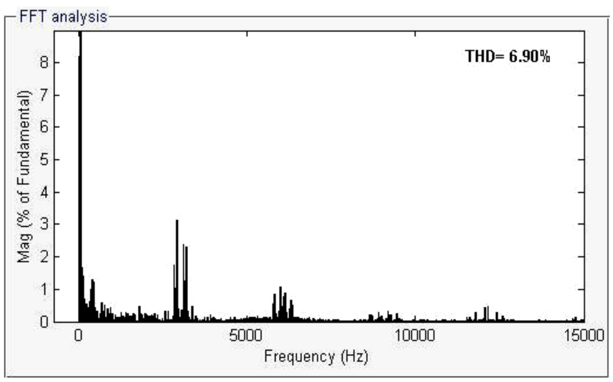

Fig. 16 THD analysis of stator current

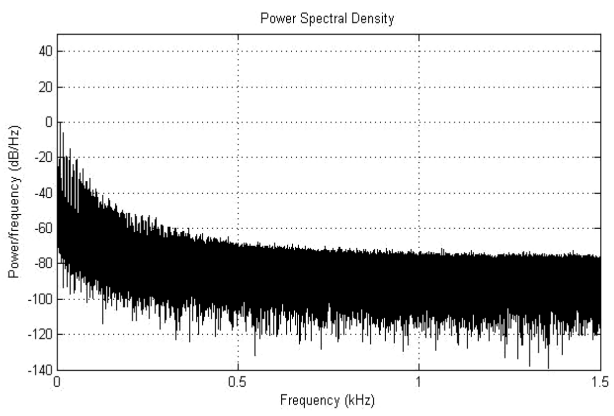

Fig. 17 Acoustic noise for VDR SVPWM

E. Steady state plots of DPWMIN (With Random)

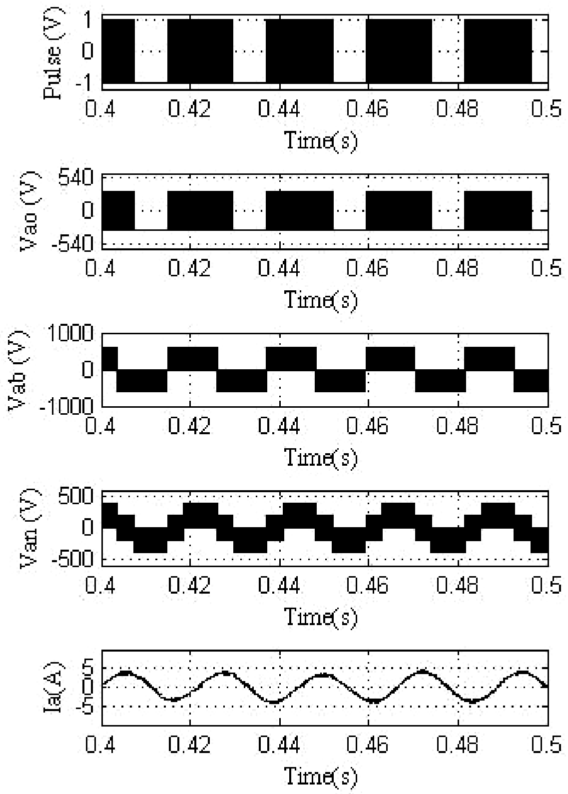

Fig. 18 Pulses, Pole voltage, Line voltage, Phase voltage and stator current

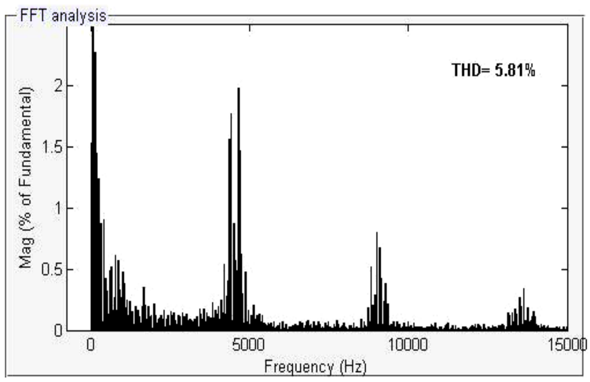

Fig. 19 THD analysis of stator current

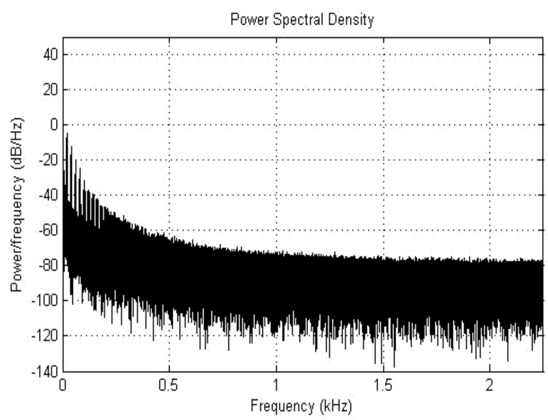

Fig. 20 Acoustic noise for VDR DPWMMIN

F. Steady state plots of DPWMMAX (With Random)

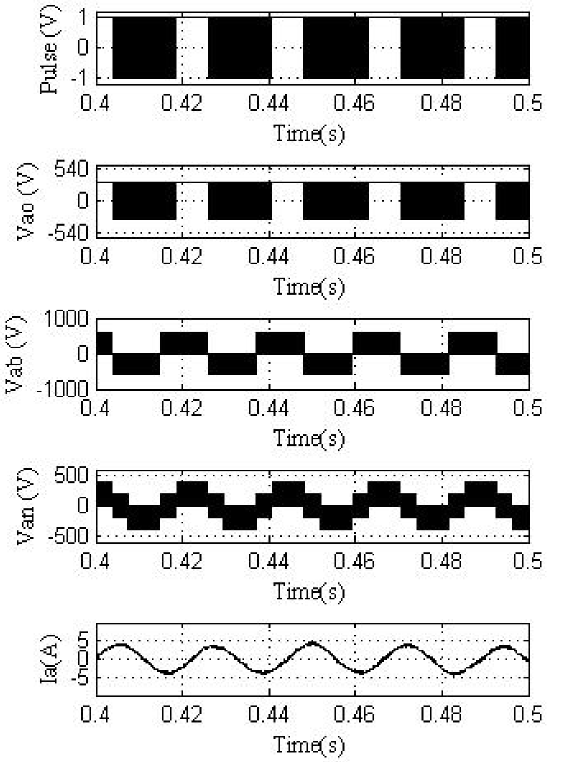

Fig. 21 Pulses, Pole voltage, Line voltage, Phase voltage and stator current

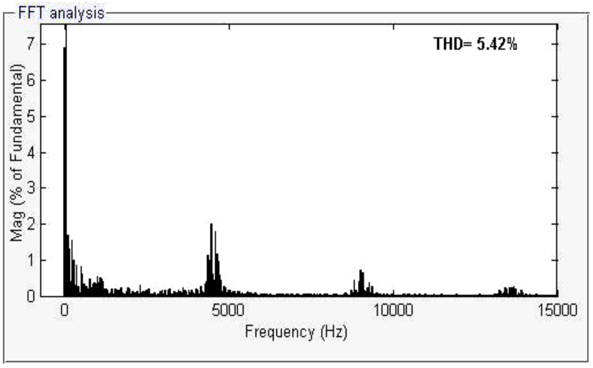

Fig. 22 THD analysis of stator current

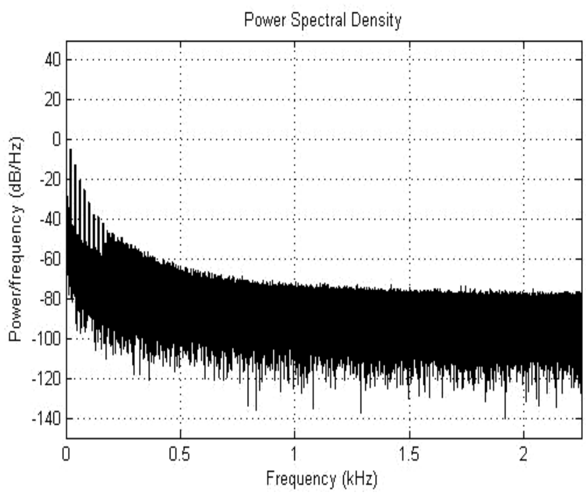

Fig. 23 Acoustic noise for VDR DPWMMAX

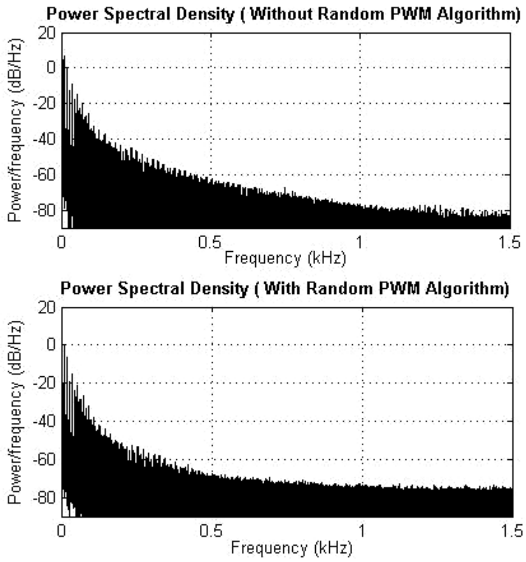

Fig. 24 Acoustic noise Comparision without and with random PWM Algorithm

6. CONCLUSION

From the simulation results, it can be observed that the proposed VDRPWM algorithms give less harmonic distortion. As the magnitude (db) of dominant harmonics is less in the proposed VDRPWM algorithms as compare to, results less acoustical noise when compared with the SVPWM algorithm. More over the proposed algorithm uses discontinuous PWM algorithms, the use of DPWM schemes reduces 33% of the switching loss of the inverter, it means that number of on and off of the inverter switch is reduced by 33% by clamping each of the pole voltage to either positive bus or negative bus for a period of 120^o.

From Fig. 24 it is observed that magnitude of acoustic noise (in db) is around -80db without random PWM algorithm but whereas for random PWM algorithm magnitude of acoustic noise is around -70 db, shows clearly that there is decrease in dominant magnitude components by using random PWM algorithm.

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